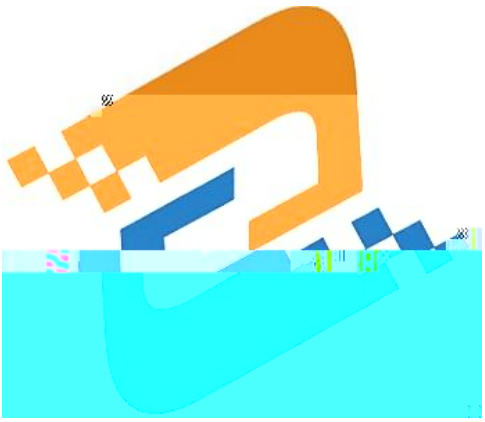

Й

- О 2.4GHz Ъ SOC
- JZRT202

:V1.0

:2019-03

JZRT202 ISM

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1
2
3 250K/1M/2M bps -91/-87/-83dBm 8dBm
4 MCU
OTP 4K×16Bit
RAM 176×8Bit
MCU 12 ADC WDT PWM

ì ²

ضم SPI ٥ Ḥ	ـ غ CRC w
ч 32 н FIFO 64 ١ FIFO	SOP16
1M / 2Mbps ±40ppm 250kbps ±20ppm	ƀ ١ 2.2~3.3V ƀ -40~+85
GFSK Ḥ	ـ ï ـ D
RSSI w	10 ɷ GPIO
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Ţ п ۋ ĭ Ţ
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ƀ ∕
17.2.1 8 β ك
17.2.2 8 β ك
17.2.3 Ð ̂ № ك
17.2.4 ض TIMER0

21.3.7 PWM ƀ

22.MCU ắ

22.1 MCUDC

22.2 MCUAC

Ɒ ₩

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1.

1.JZRT202 h

	ð (VCC = 3V±5%， TA=25)	ð ỵ			ỵ β
			ĩ ỉ		
ICC	w		2		uA
	1		30		uA
	3		650		uA
	2		780		uA
	ỗ (-35dBm)		9		mA
	ỗ (-20dBm)		9.5		mA
	ỗ (0dBm)		16		mA
	ỗ (2dBm)		19		mA
	ỗ (8dBm)		30		mA
	ỗ (13dBm)		66		mA
	(250Kbps)		15		mA
	(1Mbps)		15.5		mA
	(2Mbps)		16.5		mA
f_{OP}	ƀ	2400		2483	MHz
PLL_{res}			1		MHz
f_{XTAL}			16		MHz
DR		0.25		2	Mbps
Δf_{250K}	└ Ẓ @250Kbps		125	150	KHz
Δf_{1M}	└ Ẓ @1Mbps		160	300	KHz
Δf_{2M}	└ Ẓ @2Mbps		320	550	KHz
FCH_{250K}	@250Kbps		1		MHz
FCH_{1M}	@1Mbps		1		MHz
FCH_{2M}	@2Mbps		2		MHz
	ỗ				
PRF	ĩ ỉ ₣ w	2	8	8	dBm
PRFC	₣ w ớ	-35		8	dBm
PBW1	ỗ └ 20dB 250Kbps		500		KHz
PBW2	ỗ └ 20dB 1Mbps		1		MHz
PBW3	ỗ └ 20dB 2Mbps		2		MHz

1

RX_{max}	<0.1%		0	dBm
RXSENS1	@250Kbps		-91	dBm
RXSENS2	@1Mbps	0.1%BER	-87	dBm
RXSENS3	@2Mbps	0.1%BER	-83	dBm

C/I_{CO}		@250kbps	2	dBc
C/I_{1ST}	1	@250kbps	-8	dBc
C/I_{2ND}	2	@250kbps	-18	dBc
C/I_{3RD}	3	@250kbps	-24	dBc
C/I_{4TH}	4	@250kbps	-28	dBc
C/I_{5TH}	5	@250kbps	-32	dBc
C/I_{6TH}	6	@250kbps	-35	dBc
C/I_{CO}		@1Mbps	10	dBc
C/I_{1ST}	1	@1Mbps	1	dBc
C/I_{2ND}	2	@1Mbps	-18	dBc
C/I_{3RD}	3	@1Mbps	-23	dBc
C/I_{4TH}	4	@1Mbps	-28	dBc
C/I_{5TH}	5	@1Mbps	-32	dBc
C/I_{6TH}	6	@1Mbps	-35	dBc
C/I_{CO}		@2Mbps	10	dBc
C/I_{1ST}	1	@2Mbps	-6	dBc
C/I_{2ND}	2	@2Mbps		

2. ỵ

2.JZRT202 ỵ ỵ

ắ	ð		ٹ ﺳ		١ β
	١ ˪	-0.3		3.6	
	١ ˜	-0.3		3.6	
	١ ₣	VSS		VDD	
	(TA=-40 ~85) ẇ			300	mW
	ƀ	-40		85	
	Ũ	-40		125	

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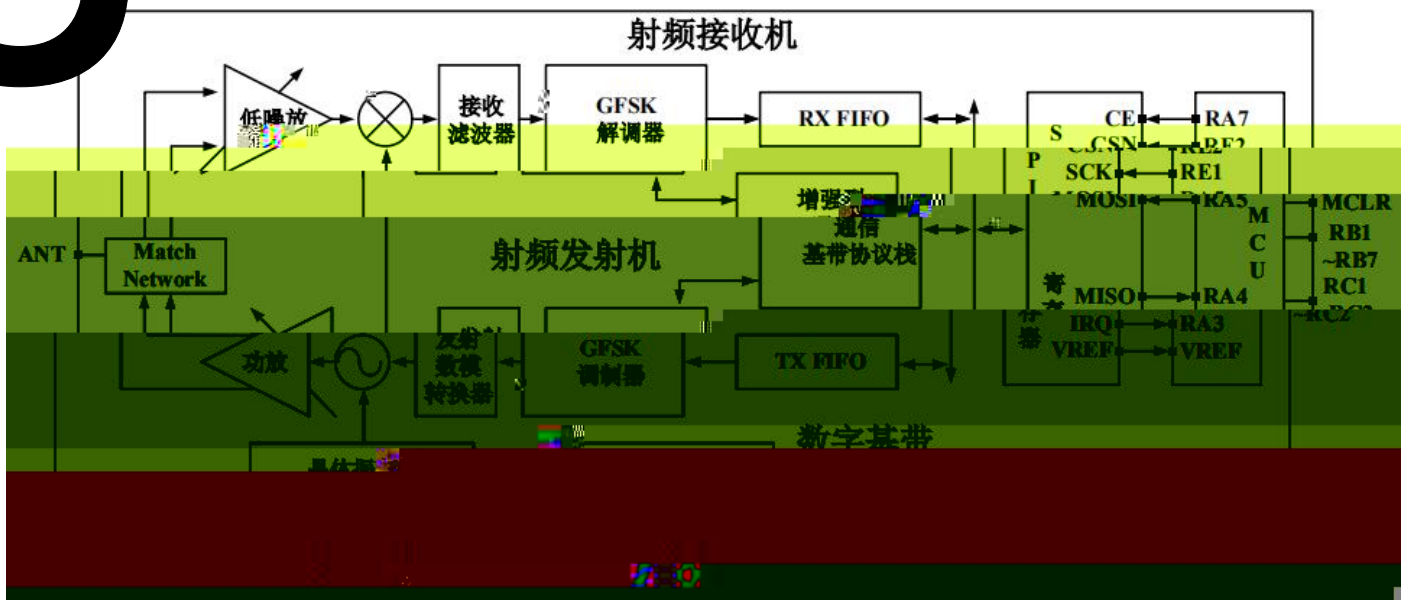
3. ỿ



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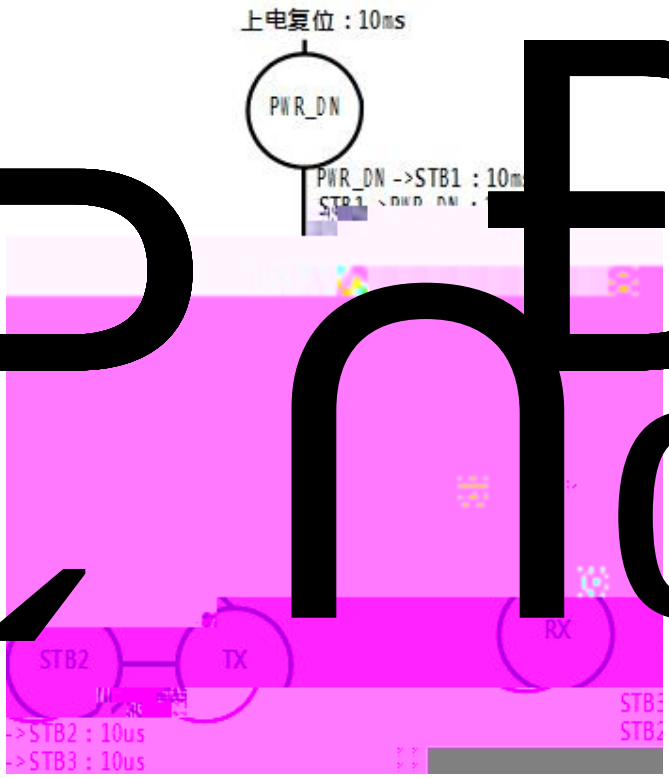
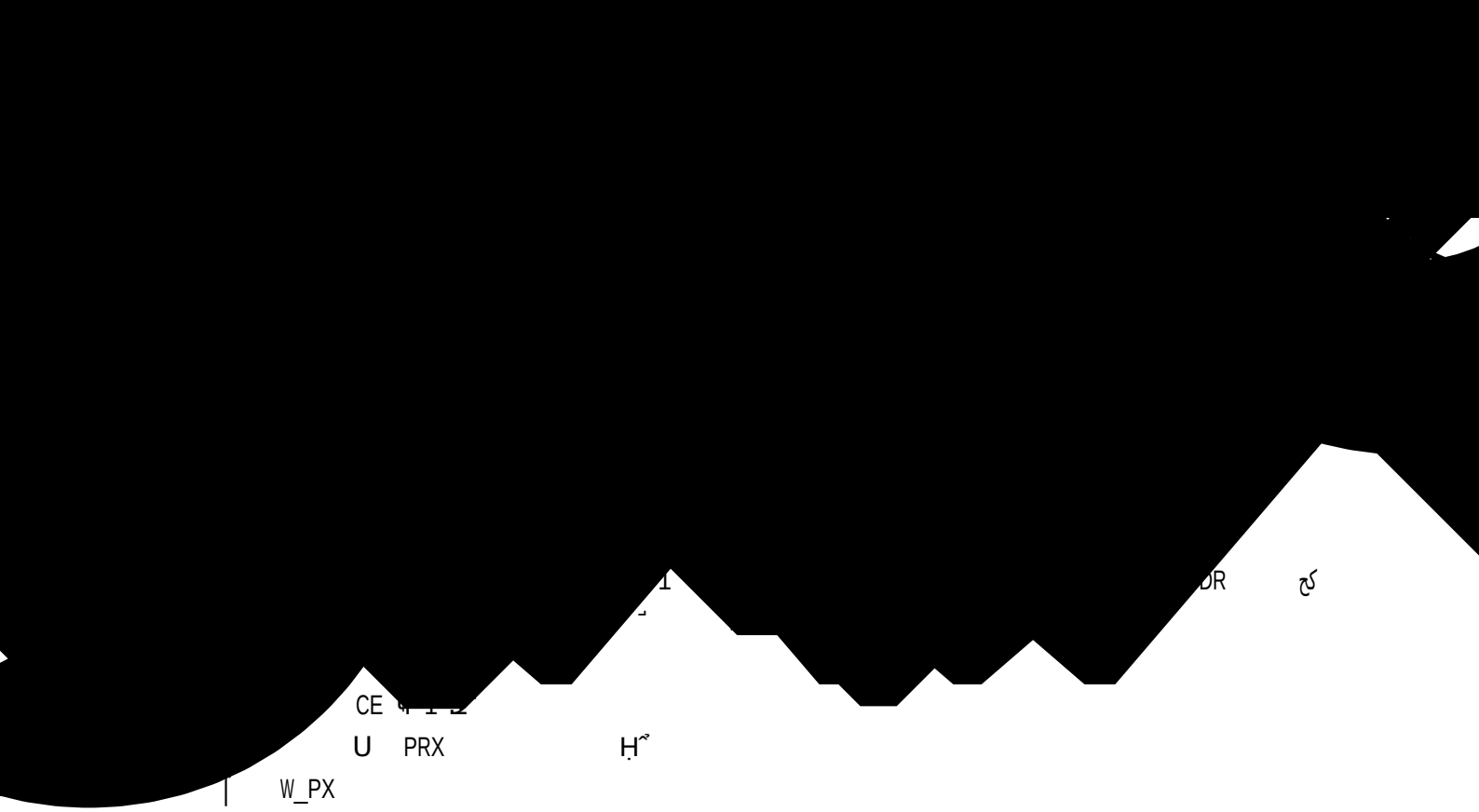
1	GND	P	


上电复位：10ms
PWR_DN
PWR_DN ->STB1 : 10m
STB2
TX
RX
->STB2 : 10us
->STB3 : 10us

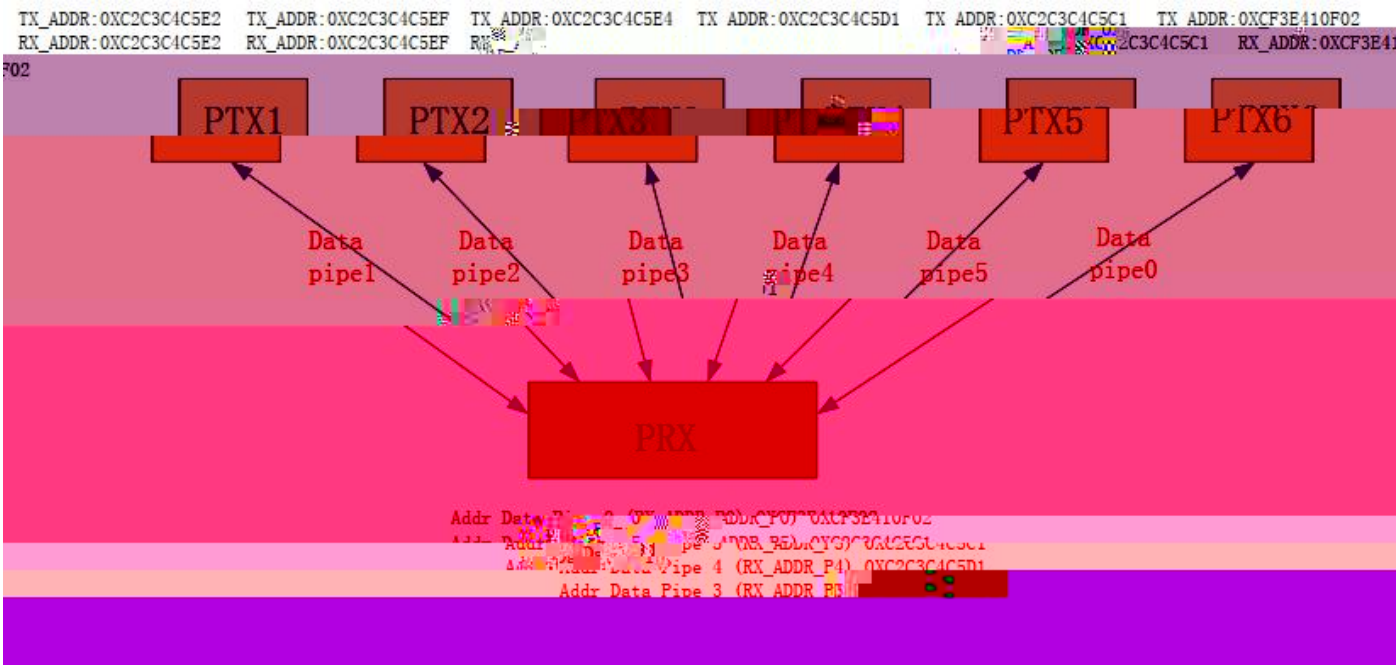
ضw Й JZRT202 w ˜ Ğ ˜w U JZRT202 Å
ƀ p ك ṗ Ğ Ь Ǐ w ك Ţ PWR_UP β L

5.2 -I STB1

ض -I Й p Ь Ŧ ỉ ﺵﺟ ỉ φ w ﺵﺟﺵﺟ ˜ ضw

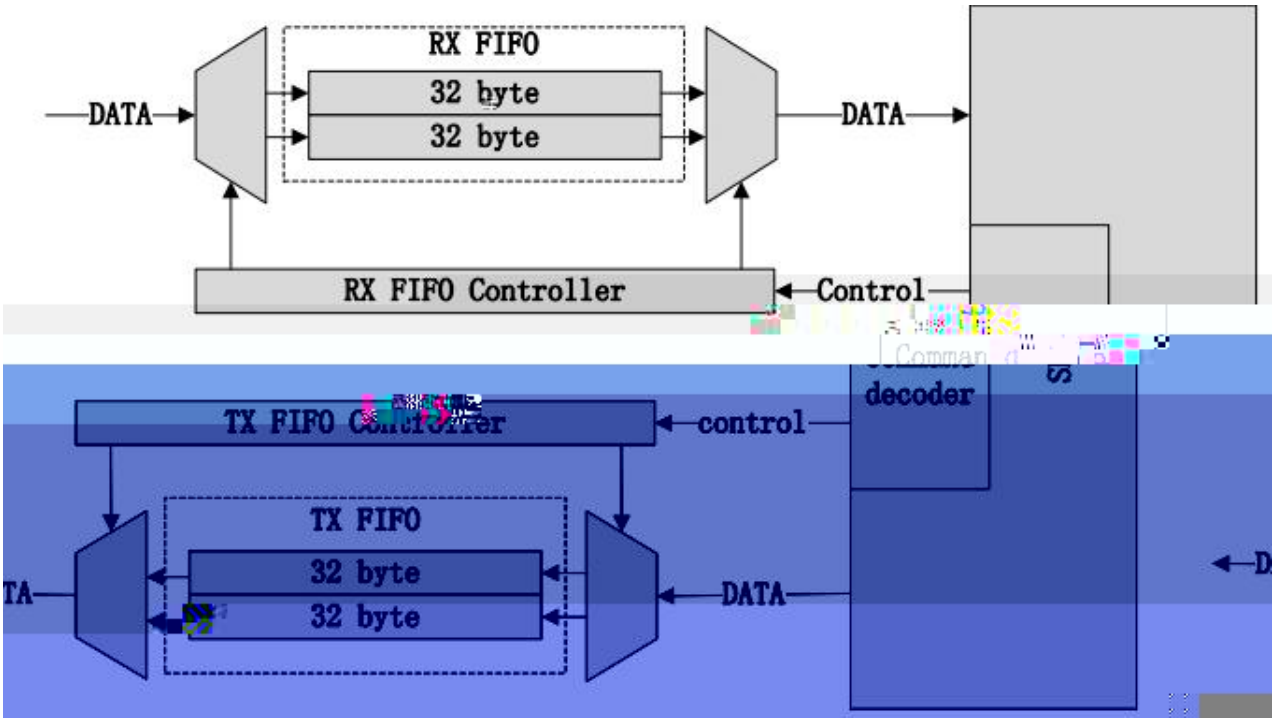

DR
CE
U PRX
W_PX

6.6



ﻱﺪ 6. D ﺥﻱﺽ ﺩ

6.8 DATA FIFO



ﻱﺪ 7.FIFO ﻱﺪ

JZRT202´ Ƈ ŭ TX_FIFO,RX_FIFO SPI ث ƥ˜ Ώ FIFO ﺽﻱ ŭ Ѝ W_TX_PAYLOAD غ W_TX_PAYLOAD_NO_ACK ƥ Ώ TX_FIFO ˚˚ MAX_RT Ţ ﺽﻱ TX_FIFO Ţ Ь Ψ ﺽﻱ Ѝ R_RX_PAYLOAD ƥ ŭ RX_FIFO Ţ payload R_RX_PL_WID ƥ ŭ payload FIFO_STATUS ƙ FIFO

6.9 Ţ

JZRT202 Ţ IRQ ч ϒ ŭ IRQ Δ ч ƙ Ţ TX_DS RX_DR MAX_RT ч 1 ϒ ĭ Ţ ą β ч 0 IRQ Ţ ŭ MCU Ţ Ώ ‘1’

Ţ IRQ Ţ ŭ ˆ ϒ ą Ţ ą β ч 1 IRQ Ţ ŭ

7.SPI L o

JZRT202 SPI L o ϔ ϛ Ώ ƀ JZRT202 ƀ ч ɾ SPI o ₩ ŭ _ G MCU o ì D ч 4Mbps ч ϶ ضw غ - SPI D ч 1Mbps

SPI o ‰ SPI o 8 ˆ ϒ ą MCU I/Oo SPI o CSN ч 0 SPI o Ɒ ₩ CSN 1 ⌈ 0 ĩ ₩ Ɒ ضCSN 1 ĩ 0 Uˆ ϒ MISO ŭ ϛ ṗ

9.SPI o

O I/O o	h	SPI	w
CSN	~	ą ϒ	ą
SCK	~		
MOSI	~	¥	~
MISO	₮	¥	₮

7.1 SPI ф

11.SPI ф

<ф ч β ⌠ γ β >

< γ ⌠ ₩ β ضي ╠>

ч ф O	ч ф ʜ∪ L	U	ƀ
R_REGISTER	000A AAAA	1 to 5 γ ضي ╠	كح AAAAA=5bit خي ضر كح
W_REGISTER	001A AAAA	1 to 5 γ ضي ╠	Ώ كح AAAAA=5bit خي ضر كح ضي w غ -I Ӣ
R_RX_PAYLOAD	0110 0001	1 to 32/64 γ ضي ╠	ƀ 0 U ɾ RXFIFO Ţ – Ӣ
W_TX_PAYLOAD	1010 0000	1 to 32/64 γ ضي ╠	Ώ ŭ Ώ ƀ 0
FLUSH_TX	1110 0001	0	TX FIFO
FLUSH_RX	1110 0010	0	RX FIFO
REUSE_TX_PL	1110 0011	0	ضي PTX Ṕ ą U ₩ ŭ ғ ŭ ч ضي ↨ ŭ FLUSH_TX ч ф Ư ф ƀ̂ γ ضي ŭ Ţ ą
ACTIVATE DEACTIVATE	0101 0000	1	ч ф U 0x73 γ Ӣ w R_RX_PL_WID W_TX_PAYLOAD_NOACK W_ACK_PAYLOAD ч ф ضي w غ Ӣ ч ф U 0x8C w
R_RX_PL_WID	0110 0000	0	RXFIFO RX-payload
W_ACK_PAYLOAD	1010 1PPP	1 to 64 γ ضي ╠	Rx ̂ Ώ PIPE PPP PPP ν ɾ 000 ⌠ 101 ڑ ACK □ ﻉ D ̂ 2 ѡ ACK ´ □ PIPE γ ۋ ۋ ₣ ﾉ ↕ ŭ Ώ ƀ ɾ 0
W_TX_PAYLOAD_ NOACK	1011 0000	1 to 32/64 γ ضي ╠	Ώ ŭ Ώ ƀ 0 TX Ӣ ą ч ф ŭ ƀ ∞ ˉ
CE_FSPI_ON	1111 1101	1	SPI ч ф ą CE ṗ 1 ч ф U 0x00

CE_FSPI_OFF	1111 1100	1	SMI

12.SPI b

					ą β
	PWR_UP	1	0	R/W	1: POWER_UP 0: POWER_DOWN
	PRIM_RX	0	0	R/W	RX/TX L β 1: PRX 0: PTX
01	EN_AA Enhanced Burst				ą EN_AA Ь ч 0X00 ч
	Reserved	7:6	00	R/W	Only 00 allowed
	ENAA_P5	5	0	R/W	ą pipe5 ¬
	ENAA_P4	4	0	R/W	ą pipe4 ¬
	ENAA_P3	3	0	R/W	ą pipe3 ¬
	ENAA_P2	2	0	R/W	ą pipe2 ¬
	ENAA_P1	1	0		

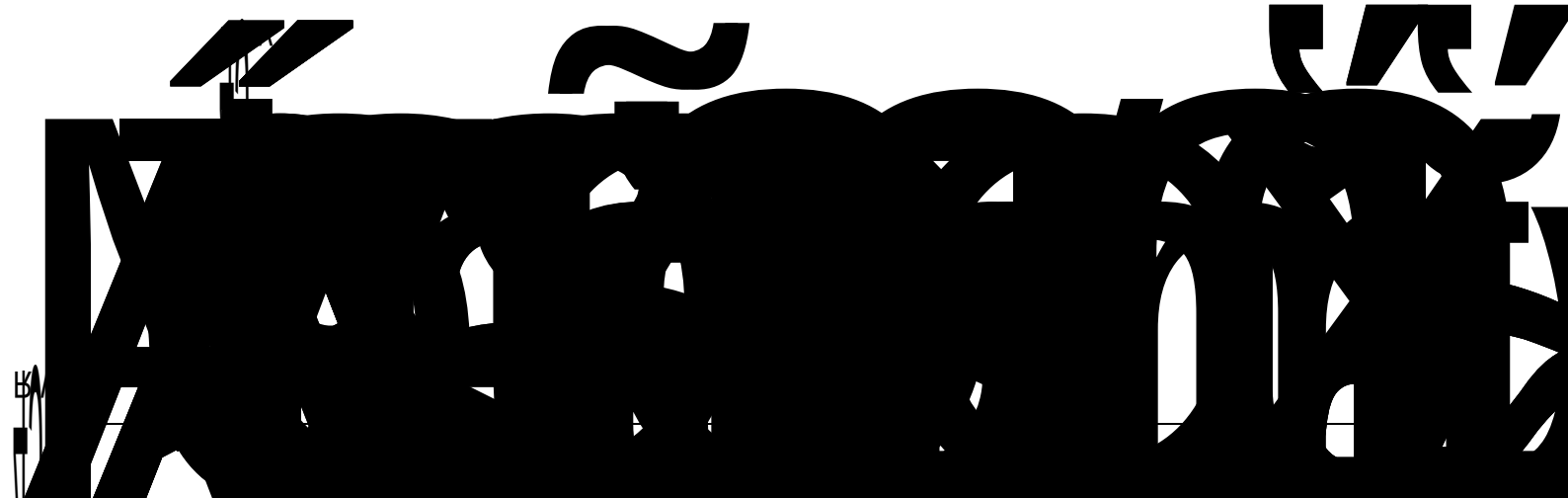
02	EN_RXADDR				ą	
	Reserved	7:6	00	R/W	Only 00 allowed	
	ERX_P5	5	0	R/W	ą	data pipe 5
	ERX_P4	4	0	R/W	ą	data pipe 4
	ERX_P3	3	0	R/W	ą	data pipe 3
	ERX_P2	2	0	R/W	ą	data pipe 2
	ERX_P1	1	0	R/W	ą	data pipe 1

09*	DATAOUT				DATAOUT_SEL=0
	ANADATA7	7	0	R	RSSI 3
	ANADATA6	6	0	R	RSSI 2
	ANADATA5	5	0	R	RSSI 1
	ANADATA4	4	0	R	RSSI 0
	ANADATA3	3	0	R	RSSI 3
	ANADATA2	2	0	R	RSSI 2
	ANADATA1	1	0	R	RSSI 1
	ANADATA0	0	0	R	RSSI 0
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	data pipe 0 5 SETUP_AW
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	data pipe 1 5 SETUP_AW
0C	RX_ADDR_P2	7:0	0xC3	R/W	data pipe 2 RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	data pipe 3 RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	data pipe 4 RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	data pipe 5 RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	PTX RX_ADDR_P0 ACK
11	RX_PW_P0				data pipe 0 RX payload
	Reserved	7	0	R/W	Only 0 allowed

RX_PW_P0	6:0	0000000	R/W	data	p

17*	FIFO_STATUS				FIFO
	N/A	7	0	R	
	TX_REUSE	6	0	R	REUSE_TX_PL W_TX_PAYLOAD W_TX_PAYLOAD_NOACK DEACTIVATE FLUSH TX
	TX_FULL	5	0	R	TX FIFO 1: TX FIFO 0: TX FIFO
	TX_EMPTY	4	1	R	TX FIFO 1: TX FIFO 0: TX FIFO
	N/A	3	0	R	
	N/A	2	0	R	
	RX_FULL	1	0	R	RX FIFO 1: RX FIFO 0: RX FIFO
	RX_EMPTY	0	1	R	RX FIFO 1: RX FIFO 0: RX FIFO
9*	DEMOD_CAL	7:0			
	CHIP	7	0	R /W	1: 0:
	CARR	6:5	00	R/W	11: CHIP 1 00:
	GAUS_CAL	4:1	0111	R/W	1111: …. 1000: …. 0000:

N/A	47:46	01	R/W	G
BW_500K	45	0	R/W	৫ 0 1
GC_500K	44	1	R/W	৫ 0 ৲ 1
IRQ_inv_sel	43	0	R/W	IRQ EN_PA ₣ ϩ ŭ ĭ 1 ₣ ŭ ĭ 0 ₣’



					ą β ~ -II Ψ ą DVDD LDO ң ì φ LDO ₩ 1: ą 0: Ь ą
	BPF_CTRL_BW	32	0	R/W	Ţ ල 1dB 1: ×1 0: ×0.85
	BPF_CTRL_GAIN	31	1	R/W	Ţ ල L 1: 5dB 0: 19dB
	VCOBUF_IC	30:29	01	R/W	VCO ⌐ MIXH ⌐ ල 00: 600uA 01: 800uA 10: 1mA 11: 1.2mA
	VCO_CT	28:27	01	R/W	VCO ₰ 00: VCO 11: VCO ٧
	CAL_VREF_SEL	26	1	R/W	VCO ⌐ ă ۱ 1: 1.15V 0: 1.25V
	SPI_CAL_EN	25	0	R/W	VCO ۱ Ŭ ⌐ β ɾ 0 1 Ψ Ŭ ₩ VCO ⌐ ض ĩ Ъ ɇ ɾ ~ Ŭ И Ӟ Ψ Ŭ VCO ⌐
	PREAMP_CTM	24:22	011	R/W	PA driver 000: 399fF 100: 171fF 111: 0fF
	DA_LPF_BW	21	1	R/W	DAC 1: 0:
	RĠCTM	20:19	0 1	R/W	LNA 00: 2.45GHz 01: 2.52GHz 10: 2.59GHz 11: 2.66GHz

	RCCAL_EN	18	1	R/W	1: ą 0: Ь ą
	EN_VCO_CAL	17	1	R/W	VCO ą β 1: ą 0: Ь ą
	PRE_BC	16:14	100	R/W	000: ×1 001&010: ×1.5 100&011: ×2 101&110: ×2.5 111: ×3
	VCO_CODE_IN	13:10	1000	R/W	VCO β ضي EN_VCO_CAL ч 0 1111: 0000: ∀
	RCCAL_IN	9:4	010100	R/W	Ţ β ضي RCCAL_EN ч 0 111111: Ţ Ţ ∀ 000000: Ţ Ţ
	CPSEL	3:2	01	R/W	RX TX 00:26uA 26uA 01:26uA 52uA 10:52uA 78uA 11:78uA 104uA
	DATAOUT_SEL	1	0	R/W	ŭ β 0
	RSSI_SEL	0	1	R/W	RSSI Ḥ 1: Ḥ 0: Ḥ Ь
1B	DEM_CAL2	23:0			H ă W ą ẏ
	PIN	23:21	000	R/W	~ U ₹ PIN MIS

	EN_RX	20	0	R/W	Ղ Ь □ Ø 1: □ 0: №
	DELAY1	19	0	R/W	Ղ ą ą ˜ γ ƀ ч ŭ 1: ą 0: ŭ L
	DELAY0	18	0	R/W	ල Ղ ŋ ४ Δ Ẓ ල Ь ŋ ४ Δ Ẓ ˜ ƀ ч 1: Ь ŋ ४ Δ Ẓ 0: ŋ ४ Δ Ẓ Ӣ γ ɢ Ţ Ẓ
	TH1	17	1	R/W	ض -II Ӣ LDO DVDD LDO Ղ ą ض Ӣ ŭ ۱ ė β 1 1: ą 0: Ь ą
	PTH	16:13	0110	R/W	ල ╠ ˜ ṿ 24 β ╠ ˜ ṿ =PTH+16 1000: 24 β 0110: 22 β 0000: 16 β
	SYNC_SEL	12	1	R/W	ල 4 Ồ ŭ ₃ β 1: 3bit 0: 2bit
	DECOD_INV	11	1	R/W	╠ Ղ β ŭ ĭ ₩ 1 ą w ŭ ң 1: Ь β ŭ ĭ 0: β ŭ ĭ
	GAIN1	10:7	1110	R/W	ල Ţ ṿ ‰ 1110
	GAIN2	6:1	000101	R/W	ල Ţ ṿ ‰ 000101
	AGGRESSIVE	0	1	R/W	ල □ ۱ ˝Ң 1: 0:
1C	DYNPD				˩ PAYLOAD ą
	Reserved	7:6	00	R/W	Only 00 allowed

	DPL_P5	5	0	R/W	ą PIPE 5 ˉ PAYLOAD (EN_DPL ɨ ENAA_P5)
	DPL_P4	4	0	R/W	ą PIPE 4 ˉ PAYLOAD (EN_DPL ɨ ENAA_P4)
	DPL_P3	3	0	R/W	ą PIPE 3 ˉ PAYLOAD (EN_DPL ɨ ENAA_P3)
	DPL_P2	2	0	R/W	ą PIPE 2 ˉ PAYLOAD (EN_DPL ɨ ENAA_P2)
	DPL_P1	1	0	R/W	ą PIPE 1 ˉ PAYLOAD (EN_DPL ɨ ENAA_P1)
	DPL_P0	0	0	R/W	ą PIPE 0 ˉ PAYLOAD (EN_DPL ɨ ENAA_P0)
1D*	FEATURE	7:0		R/W	ֵ
	Reserved	7	0	R/W	Only 00 allowed
	MUX_PA_IRQ	6	0	R/W	IRQ Ḥ ֬ EN_PA Ḥ ֬ ⌈ PIN 0 IRQ Ḥ ֬ ⌈ PIN 1 EN_PA Ḥ ֬ ⌈ PIN
	CE_SEL	5	0	R/W	ą CE ث ɒ Ω 0 CE CE L 1 CE ث ɒ L
	DATA_LEN_SEL	4:3	00	R/W	11: 64byte 512bit 00: 32byte 256bit
	EN_DPL	2	0	R/W	ą ˉ PAYLOAD
	EN_ACK_PAY	1	0	R/W	ą ACK PAYLOAD
	EN_NOACK	0	0	R/W	ą W_TX_PAYLOAD_NOACK ث ɒ
1E*	RF_CAL	23:0		R/W	ă ֵ(
	EN_CLK_OUT	23	0	R/W	ṗ Ḥ ֬ 1: Ḥ ֬ ⌈ CLK_OUT PAD 2: Ь ֬
	DA_VREF_MB	22:20	101	R/W	DAC ă ˥ ă ˥ DAC ֬ 111: ă ˥ 000: ă ˥
	DA_VREF_LB	19:17	110	R/W	DAC ă ˥ ă ˥ DAC ֬ 111: ă ˥ 000: ă ˥

	DA_LPF_CTRL	16	1	R/W	DAC Ŧ L β 1: Ŧ ×0.8 Ò 0: Ŧ ×0.5 Ò

RSSI_EN	15	0	R/W	RSSI ą β 1: RSSI ą 0: RSSI Ь ą
RSSI_Gain_CTR	14:13	01	R/W	RSSI Ḥ ⁞ β 00: Ь ⁞ 01: -6dB 10: -12dB 11: -18dB
MIXL_GC	12	1	R/W	MIXL 1: 14dB 0: 8dB
PA_BC	11:10	11	R/W	PA Ŧ β 00: ×1 01: ×

‘ J

8dB

’

	LNA_HCURR	2	1	R/W	LNA ą 1: 0: ¥

					2Mbps Й¦ RX_ACK_TIME×16 ч β ч us 1Mbps Й¦ RX_ACK_TIME×32 ч β ч us 250kbps Й¦ RX_ACK_TIME×128 ч β ч us

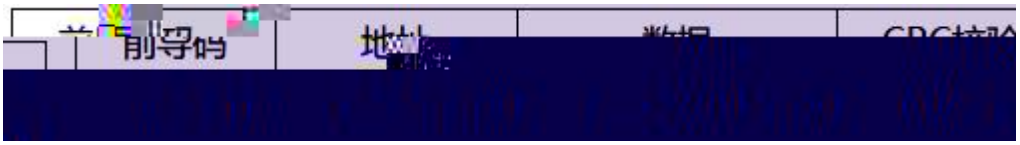
1 13 ч 0X1B 0X1F кй ўˆ ץ ƀ' 0X19 0X1A 0X1E кй ч кй
2 кй /خي ضر/ /Ω ч ץ ضي ╠ ضي U ч ¢ ף bit ضي ╠ ץ bit ضي U

9. ´

9.1 ´

´ 14 I

14. ´



14 Ţ غ خي ضر №ˆ ץ ą / ˜ β

9.2 ´

´ 15 III

15. ´

╠ 3	خي ضر 3~5	10bit			(0~32/64)	CRC (0/2)
		7bit	PID 2bit	NO_ACK 1bit		

9.3 ACK´

ACK´ 16 II

16. ACK´

╠ 3	خي ضر 3~5	10bit					CRC (0/2)
		7bit	PID	2bit	NO_ACK	1bit	

10.MCU

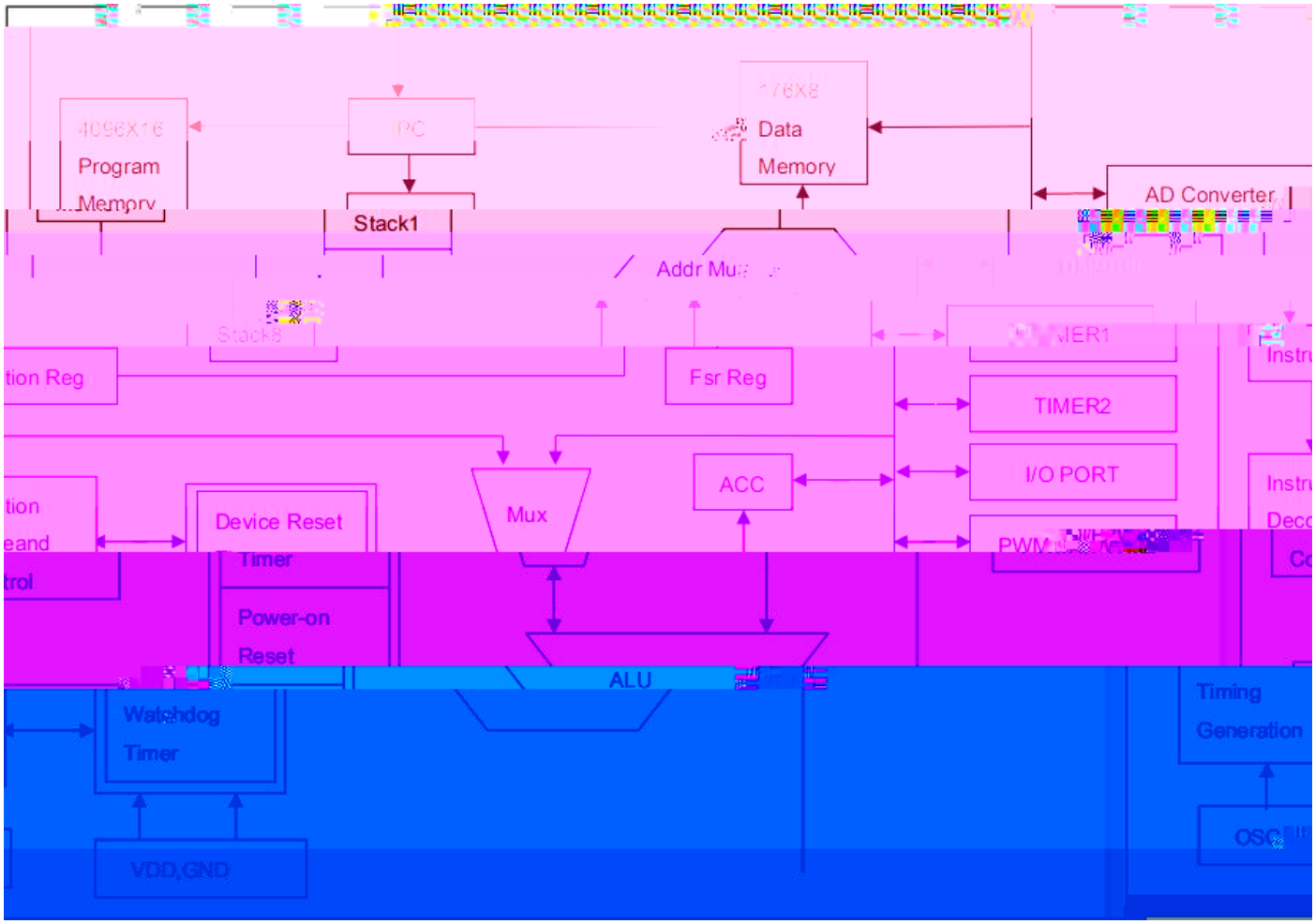
10.1

CPU
OTP 4K × 16Bit
RAM 176 × 8Bit
8
(68
)
12 ADC
WDT
PWM

2.5V—3.3V@8MHz -40 —85
2.2V—3.3V@4MHz -40 —85

3
RB
8 TIMER0 TIMER2
16 TIMER1
RC 8MHz

10.2



11.

10.3

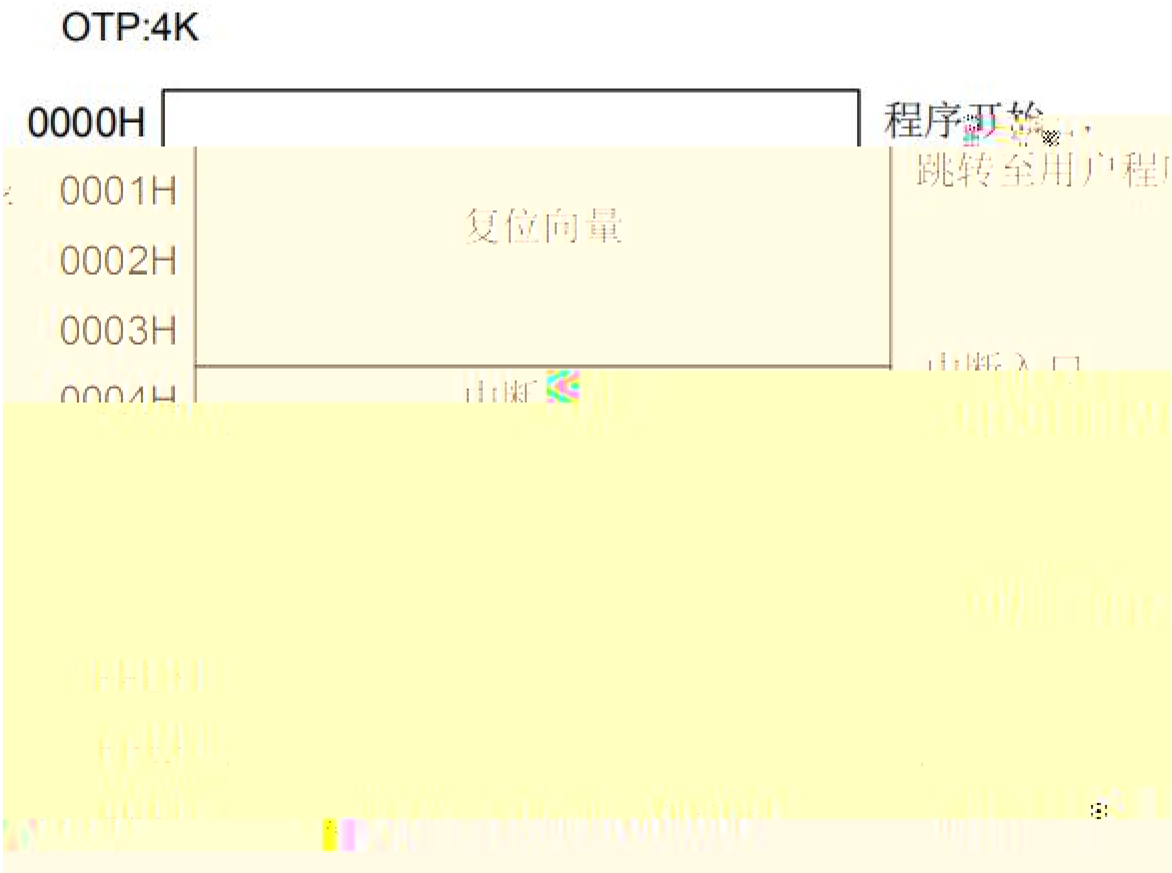
CONFIG MCU

1 OSC( )
INTRC RC
2 WDT( )
ENABLE
DISABLE
3 PROTECT( )
DISABLEOTP
ENABLEOTP
4

11. Ț ك CPU

11.1 ṗ

11.1.1 ṗ



ﻳﻰ 13.JZRT202 Ǘ ك

11.1.1.1 ᵝ h (0000H)

ɏ ỉ ẘ ɷ ᵝ h 0000H ỉ ɣ Ӂ ᵝ

ᵝ

ᵝ

ᵞ ⅎ ᵝ LVR

ΰ ҝ ẘ ᵝ U ɽ 0000H ك ӟ ҹ ỵ

STATUS ك Ț PD ع TO ᵝ ṗ ̃ ɣ ∞ ᵝ Ӂ ẘ ২ ᵥ ɧ

ROM Ț ᵝ h

ᵖ ɧ ᵝ h

```
        ORG              0000H        ᵝ h
        JP               START
        ORG              0010H
   START

        END
```

11.1.1.2 Ţ h

Ţ h ضخي ч 0004H ₩ Ţ ذ كح PC ╠ ٧ Ψ ~ كح
⌠ 0004H Ţ ⊢ Ţ Ψ ~ 0004H ѽ Ţ h ΐ ر ك ѽ
Ţ Ţ β كح β ═ Ѝ ɒ ↄ ٧ Ώ Ţ ⊢

ɒ Ч Ţ h Ţ ضي Ч U

```
        ORG     0000H       β h
        JP      START
  ORG           0004H
INT_START:
        CALL    PUSH  Ḡ  ACC  STATUS


INT_BACK:
        CALL    POP   عج ACC  STATUS
        RETI          Ţ  عج
START


        END
```

G ٦ L F ₹ ٨ Ɒ Ḡ Ţ شي

ɒ Ţ ~o Ḡ شي

```
PUSH:
    LD      ACC_BAK,A   ;Ḡ  ACC  Ч  كح ACC_BAK
    SWAPA   STATUS      ;     كح STATUS  ٢ ٦  ε
    LD      STATUS_BAK,A;Ḡ     Ч  كح STATUS_BAK
    RET                 ;  عج
ɒ Ţ ₹o شي
    POP:
      SWAPA   STATUS_BAK  ; Ḡ  STATUS_BAK  ٢ ٦  ε
                          ACC
      LD      STATUS,A    ;  ACC  ٧  كح STATUS
      SWAPR   ACC_BAK     ; Ḡ  ACC_BAK  ٢ ٦  ε
      SWAPA   ACC_BAK     ; Ḡ  ACC_BAK  ٢ ٦  ε
                        ACC
      RET               ;  عج
```

11.1.1.3

ΐ W ROM К ٧ ضخي ̂ Ạ ч ą

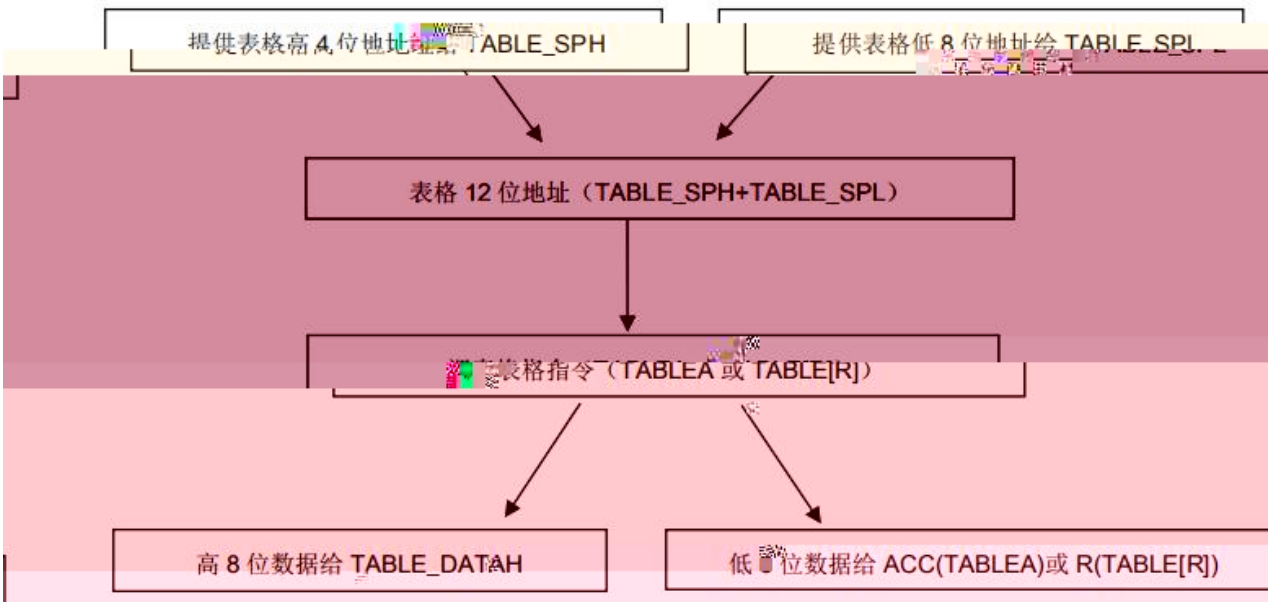
ˀ Ɒ

· TABLE [R] ṗ ٢ كح R ⌠ كح TABLE_DATAH
· TABLEA ṗ ٢ ٧ كح ACC ⌠ كح TABLE_DATAH

ˀ كح

· TABLE_SPH ̂ Ώ كح 5 β ضخي
· TABLE_SPL ̂ Ώ كح ٢ 8 β ضخي

· TABLE_DATAH



14.

…

LDIA 02H ;

╠ Ɒ U PCL ν Ψ ϕ 1 ˆ ă γ Ѝ ɒ PCL ACC U ŭ ₣ PC Ь Ψ ˉ

β Ώ ˆ γ ќ ACC ν خي ضر

PCLATH ч PC β ‖ ҫ PCL ƀ ѽ PCLATH ν

ɒ خي ضر ɒ

OTP خي ضر

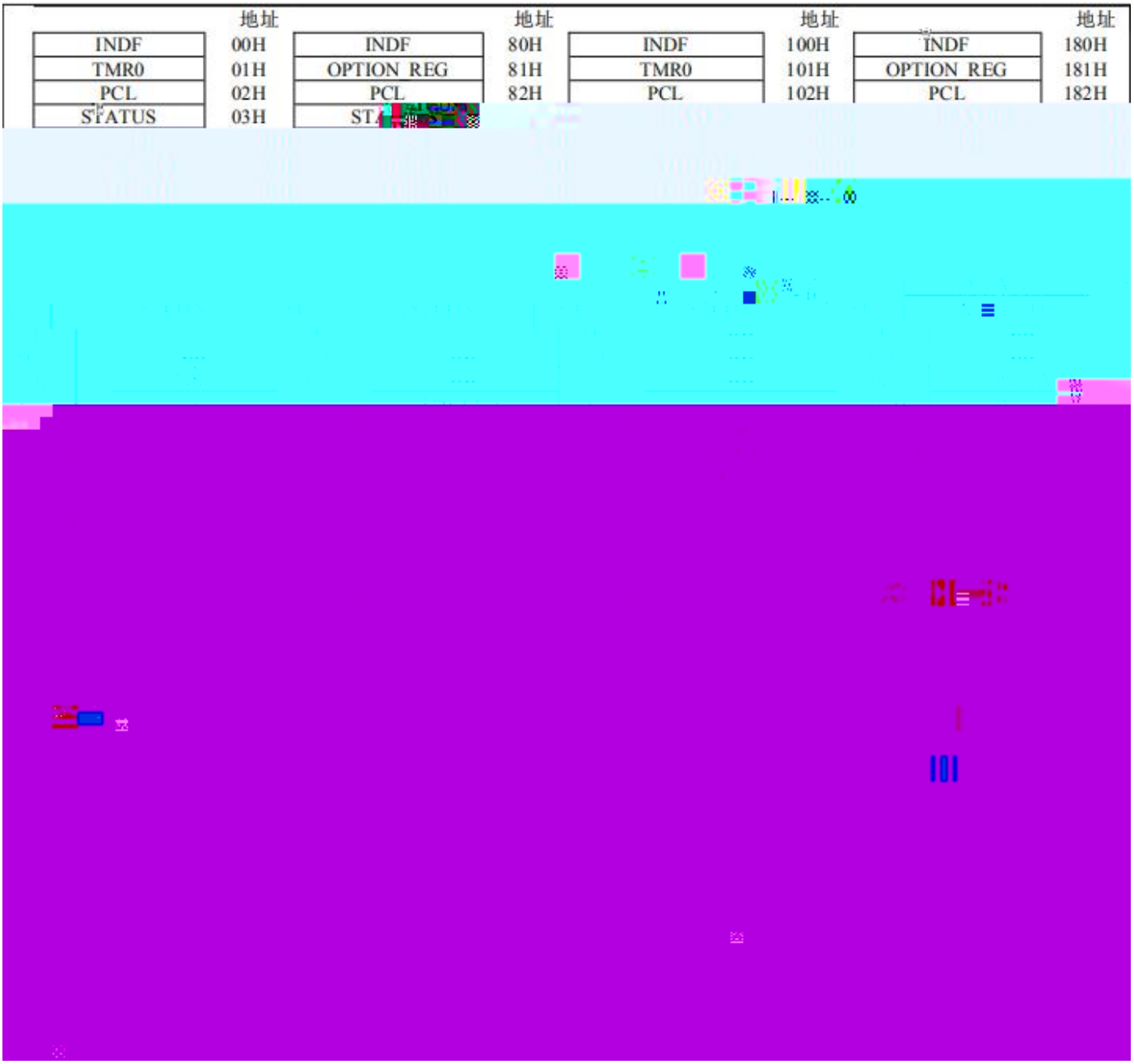
	LDIA LD	01H PCLATH,A		
			; PCLATH	ν
	…			
0110H:	ADDR	PCL	;ACC+PCL	
0111H:	JP	LOOP1	;ACC=0	LOOP1
0112H:	JP	LOOP2	;ACC=1	LOOP2
0113H:	JP	LOOP3	;ACC=2	LOOP3
0114H:	JP	LOOP4	;ACC=3	LOOP4
0115H:	JP	LOOP5	;ACC=4	LOOP5
	JP	LOOP6		

ɒ خي ضر ɒ

OTP خي ضر	CLR	PCLATH		
	…			
	ADDR	PCL	;ACC+PCL	
00FDH:	JP	LOOP1	;ACC=0	LOOP1
00FEH:	JP	LOOP2	;ACC=1	LOOP2
00FFH:	JP	LOOP3	;ACC=2	LOOP3
0100H:	JP	LOOP4	;ACC=3	0000H خي ضر
0101H:	JP	LOOP5	;ACC=4	0001H خي ضر
0102H:	JP	LOOP6	;ACC=5	0002H خي ضر

11.1.2 Ũ ك

地址		地址		地址		地址	
INDF	00H	INDF	80H	INDF	100H	INDF	180H
TMR0	01H	OPTION_REG	81H	TMR0	101H	OPTION_REG	181H
PCL	02H	PCL	82H	PCL	102H	PCL	182H
STATUS	03H	STA					



ﺓ 15.JZRT202 Ũ ك ↓

Ũ ك 512 × 8 β № ч н ɷ w ٧ w ك غ Ũ ك Ũ ك
ٮ ″Ḥ ˜ / Ω p ˢ ₇ w ك ضر خي ч ɾ 00H-1FH 80-9FH 100-11FH
180-197H

17.MCU w كح Bank2

ضخ	O	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	β ٧
00H	INDF	خي ١ "Ḥ ψ ą	FSR	ṗ	خي	Ũ' كح	ь	كح		xxxxxxxx
01H	TMR0	TIMER0	كح							xxxxxxxx
02H	PCL	كح ٧								00000000
03H	STATUS	IR P	RP1	RP0	TO	PD	Z	DC	C	00011xxx
04H	FSR	Ũ' كح ضخي								xxxxxxxx
05H	PORTA	RA7	----	RA5	RA4	RA3	----	----	----	xxx-xxx---
06H	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	----	xxxxxxx-
07H	PORTC	--- -	----	----	----	----	RC2	RC1	RC0	-----xxx
09H	PORTE	--- -	----	----	----	----	RE2	RE1	----	-----xx-
0AH	PCLATH	--- -	---	----	----	كح 4 β Ω ‖ كح				----0000
0BH	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	00000000
0CH	PIR1	--- -	ADIF	----	----	----	----	TMR2IF	TMR1IF	-0---000
0EH	TMR1L	16 β TIMER1	كح ٧		كح					xxxxxxxx
0FH	TMR1H	16 β TIMER1	كح		كح					xxxxxxxx
10H	T1CON	----	----	T1CKPS1	T1CKPS0	----	----	----	TMR1ON	--00---0
11H	TMR2	TIMER2	شد كح							00000000
12H	T2CON	----	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0				

ɔ'0(ɔ

0

خي ضر	O	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	β ٧
80H	INDF			خي ضر ١ خي "Ḥ Ψ ą	FSR	ṗ	خي	Ũ ك	ь	ك	xxxxxxxx
81H	OPTION_REG	RBPU	INTEDG	T0CS	T0SE		PSA	PS2	PS1	PS0	11111111
82H	PCL		ك PC	٧							00000000
83H	STATUS	IRP	RP1	RP0	TO		PD	Z	DC	C	00011xxx
84H	FSR		Ũ خي ضر ك								xxxxxxxx
85H	TRISA	----	----	----	TRISA4	TRISA3	TRISA2	----	----		---111--
86H	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	----		1111111-
87H	TRISC	----	----	----	----	----	TRISC2	TRISC1	----		-----11-
89H	TRISE	----	----	----	----	----	TRISE2	TRISE1	----		-----11-
8AH	PCLATH	----	----	----	----			ك 4 β Ω ك Ⅱ			----0000
8BH	INTCON	GIE	PEIE	T01E	INTE	RBIE	T0IF	INTF	RBIF		00000000

18.MCU w Bank3

ضي	O	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	β ٧
180H	INDF	ي ضي ١ "Ĥ Ψ ą		FSR	ṗ	ي	Ũ' ك	ƀ	ك	xxxxxxxx
181H	OPTION_REG	RBPU	INTEDG		T0CS	T0SE	PSA	PS2	PS1	PS0 11111111
182H	PCL	PC ٧								00000000
183H	STATUS	IRP	RP1		RP0	TO	PD	Z	DC	C 00011xxx
184H	FSR	ي ضي ك Ũ'								xxxxxxxx
186H	TRISB	TRISB7	TRISB6		TRISB5	TRISB4	TRISB73	TRISB2	TRISB1	---- 1111111-
18AH	PCLATH	----	----		----	----		ك 4 β Ω ك		----0000
18BH	INTCON	GIE	PEIE		T01E	INTE	RBIE	T01F	INTF	RBIF 00000000

11.2 ي

11.2.1 ي

ƀ ك ACC RAM ƀ

ɒ ACC ٧ 30H ك

ɒ 30H ك ٧ ACC

11.2.2 ٧ ي

٧ D ƀ ك ACC

ɒ ٧ 12H ACC

11.2.3 ي

Ũ' ك ي INDF ك ي INDF ƀ ك

INDF ŭ Ψ FSR ك ṗ ٧ ٧ 8 β غ STATUS ك IRP β 9 β

ƀ ٩ ضي h ضي ك غ ض ح FSR ك غ STATUS ك IRP β U

INDF ك ƀ ك ŭ ŭ INDF FSR=0 00H Ω ~ INDF

ك ŵ ɷ ƀ γ Й ɒ ح Ţ ي

ɒ FSR ĭ INDF

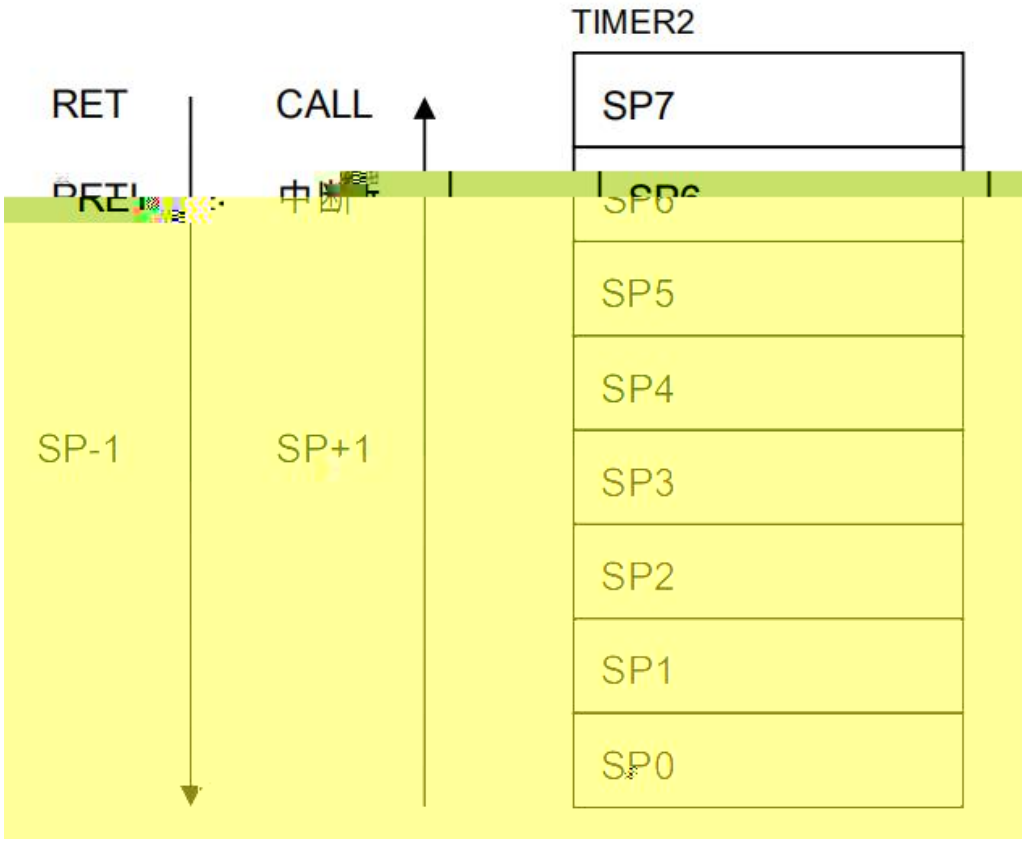
```
        LDIA    30H
        LD      FSR,A       ;   ي   h 30H
        CLRB    STATUS,IRP  ;   9 β
        CLR     INDF        ;   INDF    FSR h 30H ضي
                            RAM
```

ɒ ي RAM(20H-7FH) ɒ

```
        LDIA    1FH
        LD      FSR,A           ;间接寻址指针指向 1FH
        CLRB    STATUS,IRP
LOOP:
        INCR    FSR             ;地址加 1，初始地址为 30H
        CLR     INDF            ;清零 FSR 所指向的地址
        LDIA    7FH
        SUBA    FSR
        SNZB    STATUS.Z        ;一直需要清零 FSR 地址到 7FH
        JP      LOOP
```

11.3

ϵ ˜ 8 ϵ Ь Ũ ϵ ϖ № Ӟ Ь ṗ ϖ №
ғ Ь ǂ Ӟ Ь Ώ ˜ ƀ SP SP Ӟ Ь
ǂ Ώ ˜ β U Ψ h ΰ ΐ Ţ ϵ PC
ν ʌ ˜ ϵ ɾ Ţ ϰ ν ϰ ϵ PC , Ѝ ϰ ì ƀ ʌ



ϰ 16. Ь ʌ

ϵ ą ϖ ɷ ʌ ↕ “ ώ U ǂ ”

ϵ7 ғ ΰ Ь Ţ Ӈ7 Ţ β Ψ
Ѝ Ţ ŭ ↕ Ψ L ∫ ΰ ⋮ Ţ Ψ ŭ ɷ W ˜ Ƴ
Ţ ą ǂ ▯ ғ ΰ Ӈ Ψ ΰ ǂ ώ
˜ ṗ Ψ ϗ 7 U ɷ ﻍ ﺽ ﻍ Ḡ ﺽ Ώ Ƴ
ϔ ΰ

11.4 Ь ϵ ACC

11.4.1

ALU 8Bit MCU

STATUS

ACC 8Bit ALU CPU ALU

11.4.2 ACC

ACC

```
LD   A,R01   ; R01 ACC
LD   R02,A   ; ACC R02
```

ACC

```
LDIA  30H   ;给 ACC 赋值 30H
ANDIA 30H   ;将当前 ACC 的值跟立即数 30H 进行“与”操作，
            ;结果放入 ACC
XORIA 30H   ;将当前 ACC 的值跟立即数 30H 进行“异或”操作，
            ;结果放入 ACC
```

ACC

```
HSUBA R01   ;ACC-R01   ACC
HSUBR R01   ;ACC-R01   R01
```

ACC

```
SUBA  R01   ;R01-ACC   ACC
SUBR  R01   ;R01-ACC   R01
```

11.5 (STATUS)

STATUS

1 ALU

2

3 GPR SFR

STATUS Z DC C

STATUS 1

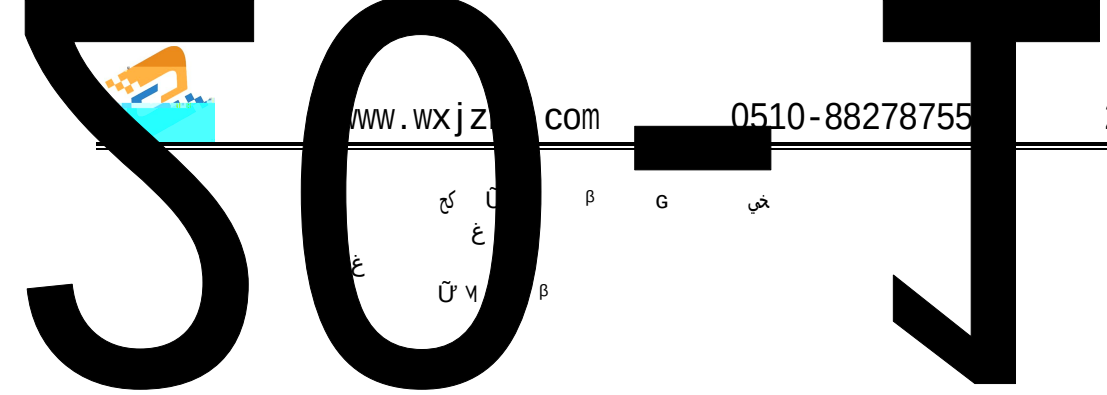
TO PD STATUS

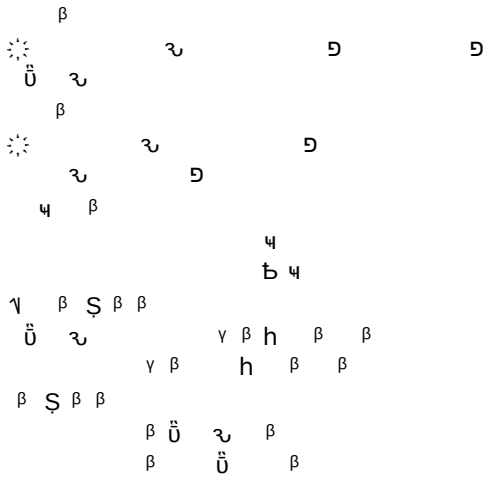
CLR STATUS 3 Z 1 STATUS 000uu1uu =

CLRB SETB SWAPA SWAPR STATUS

19. STATUS 03H

03H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	1	1	X	X	X





TO PD TO PD TO PD TO PD

20-1. PD

TIMER0 WDT ą № ל ŋ ɒ L ˆ ץ˙ ĭ ч ъ ѽ ѫ Ь
β ɾ TIMER0 ч WDT ą ץ Й ɒ

№ ל ɾ № Ⓟ ч № ﺷ ץ Й ɒ

```
CLRWDT                          ;WDT
LDIA        B'00xx0xxx'         ;       № ל
LD          OPTION_REG,A
```

ą ŭ № ˆ ל β № ל №

11.7 ל

WDT Ь TIMER0 ˜ 8 β № ϲϰ ضي β U WDT ₣ Ա 18ms Ẋ ₦ ĩ
WDT Ա ˆ ϒ OPTION_REG ϲϰ WDT ₣ Ա ỉ ⌠ ۷ ă
ڑ

“ CLRWDT ” ė “ STOP ” Ɒ WDT ϲϰ ϒ ĭ № ϲϰ ν № ϲϰ №
WDT WDT ₩ ˆ ϒ ۷ ضي ’ Ѝ
WDT ضي ỉ ₣ ╠ “ CLRWDT ” Ɒ ϒ ℃ β G
Ꮋ Ь ضي WDT ₣ ╠ “ CLRWDT ” Ɒ Ψ ą WDT ₣ ℃ β ą Ω Ь
G ˇ L WDT ₣℃ β ↕ ϲϰ STATUS “ TO ” β Ψ ˆ
β ∞ β Ղ WDT ₣

1. ą WDT ᴡ ₩ ضي ˢ ضر “ CLRWDT ” Ɒ ϒ Ğ ضي WDT ₣ ╠
Ղ Ψ ą Ь Å β ƀ
2. Ь ضي Ţ Ţ WDT Ղ ↕ ᵸ ⌠ h “ ” ’
3. Ţ ضي h Ţ ₩ WDT ƀ Ь ضي ⓠ № Ţ WDT
Ű ϲϰ Ğ ᴡ
4. ϲϰ Ь ▯ ₣ ₩ ϒ WDT Ь WDT ₣
Ό φ ϒ ѽ ₣ Ь WDT β

11.8.2 ϲϰ L ϲϰ WDTCON

22. ϲϰ L ϲϰ WDTCON(105H)

105H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	----	----	----	----	----	----	----	SWDTEN
R/W	----	----	----	----	----	----	----	R/W
β ν	----	----	----	----	----	----	----	0

Bit7-1 ч 0
Bit0 SWDTEN Ð ą ϲϰ β
1= ą WDT
0= WDT β ν

Ţ β ↕ ą Ь L β ˜
Ţ β ↕ˆ ϒ ą L β ą

12.

12.1

Ḥˆ ṗ ℃ ضي ṗ℃ 4 ⓠ Ŋ ´ Ḥˆ №≠ ƀ Q1 Q2 Q3 Q4
ضي IC ṗ ⓠ Q1 ą ϲϰ PC ѵ ₩ Q4 ɾ Ũ ٧ ″Ḥ Ţ ŭ ₣ Ɒ ỉ
ضي Ɒ ϲϰ Ţ ضي Ѝ ₩ ⓠ
Q1 ⌠ Q4 ң ŭ ₣ Ɒ ė Ӟ 4 ⓠ Ա Ψ ₩ Ɒ Ѝ
ᴝ Ь Ɒ Ա ᴝ

13.2.2 β W

ν β γ Й Ŧ з

ɻ ↑ G β ˜

Ƣ ᴄᴋ

ʏ ƀ

ɻ Й

ᴄᴋ

ᴄᴋ G Ḡ ˜ ƀ Ɱ Ŧ ᴄᴋ

Ψ Ŧ β

ʏ ƀ

ƀ ʏ ƀ ɻ ɾ ᴤ ƀ Ɱ ɦ ʏ ƀ

˜ γ ʏ ʏ ƀ ɻ ɾ ⋮ ƀ ض Ɱ ɻ

ɻ Й

˜ G ƀ ض ᴸ ₩ ᴸ ɻ ض Ţ Й

Ψ ƀ ض Ɱ ɻ ƀ ˜ Ŧ

ض Ь ض ν ₩ ɷ γ Ḃ Ɱ ~ β Ɱ ѽ

Ŧ ˜

13.3 β

β ₩ Ḡ ض Й ᴄᴋ Ŧ

G ᴄᴋ Ŧ β β U Ƣ ~

β Й

ᴄᴋ ᴄᴋ ϒ Ŧ Ŧ ↕ β’

Δ . ᴄᴋ ɥ ’

ᴄᴋ ƀ ᴄᴋ ᴸ ’

β

14. w

14.1 ˜ w

ɒ˜ ~ ą Ꮋ

’

ᴄᴋ Ţ β ’

β ’

˜ ᴄᴋ ˗ ᴄᴋ

ο Ḡ ɒ ɦ ╠ ˗ ɥ ʏ

ض w Й ɥ ᴝ ʏ Ḡ ɥ

ɾ ɥ ᴝ ѽ ~ ~ ˜ ض ~

ɥ ʏ ɥ ᴝ ʏ ṗ ڒ

14.2 ᴄ w ɨ

˜ γ Й ↓ ĸ ₩ Ꮋ ʊ ð ᴄᴋ ð ᴄ w ɨ

ᴄᴋ ɨ ᴸ ą

ỉ. Ţ Ţ

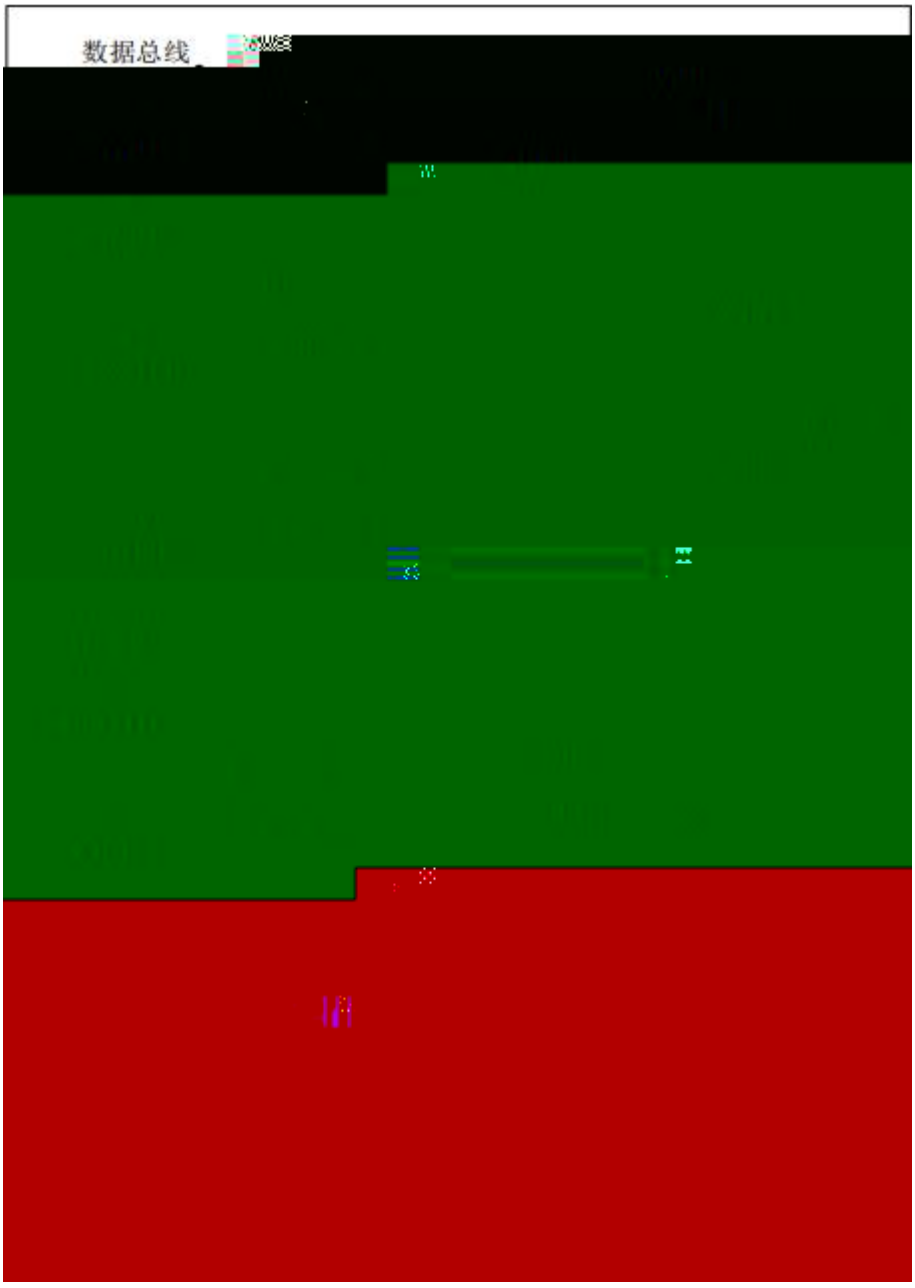


图 20.RBo

15.2 PORTB

15.2 .1 PORTB ǐ h

ẅ ɷ β ǐ h ο h ᶎ ч Ţ ɷ β

ˆ ɣ ą ƀ ч ~ Ţ ɷ β ą

ƀ ч ∓

ᶎ Ώ ᶎ Ψ Ώ ~ ο ᶎ Ώ ƀ

ḱ Ώ ƀ ɨ Ώ ẅ ɷ ο ɛ ѽ ο ḱ ⌡ ṿ U ʹP

ṿ Ώ ~ ο ᶎ

Ь ο ᶎ

15.2.2 PORTB

95H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	----
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	----
	0	0	0	0	0	0	0	----

15.3 PORTC

15.3.1 PORTC ĭ h

w ɷ β ĭ h o h ֆ ɥ Ţ ɷ β
ˆ ɣ ą ƀ ɥ ~ Ţ ɷ β ą
ƀ ɥ ǂ
ֆ Ώ ֆ Ψ Ώ ~ o ֆ Ώ ƀ
ḱ Ώ ƀ ɨ Ώ w ɷ o ɛ ώ o ḱ ⌠ ṿ U ʹP
ṿ Ώ ~ o ֆ
ֆ

07H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORTC	----	----	----	----	----	RC2	RC1	RC0
R/W	----	----	----	----	----	R/W	R/W	R/W
β ṿ	----	----	----	----	----	x	x	x

β

o
o
h ֆ

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TRISC	----	----	----	----	----	TRISC2	TRISC1	TRISC0
R/W	----	----	----	----	----	R/W	R/W	R/W
β ṿ	----	----	----	----	----	1	1	1

⁚⁚ L β
ɥ ~ ⁚⁚
ɥ ǂ

ǂ ₇ ǂ W

ɒ o

```
CLR     PORTC       ;       ֆ
LDIA    B'01110000' ;       PORTC<3:0> ɥ ǂ₀
LD      TRISC,A
```

15.3.2 PORTC⁚⁚

ɷ ˆ ɬ ṗ ⁚⁚ L β ą ɷ ⁚⁚
o ɥ ǂ ĭ ⁚⁚ Ψ ˉ Ⓟ
⁚⁚ ֆ

18FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WPUC	----	----	----	----	----	WPUC2	WPUC1	----
R/W	----	----	----	----	----			

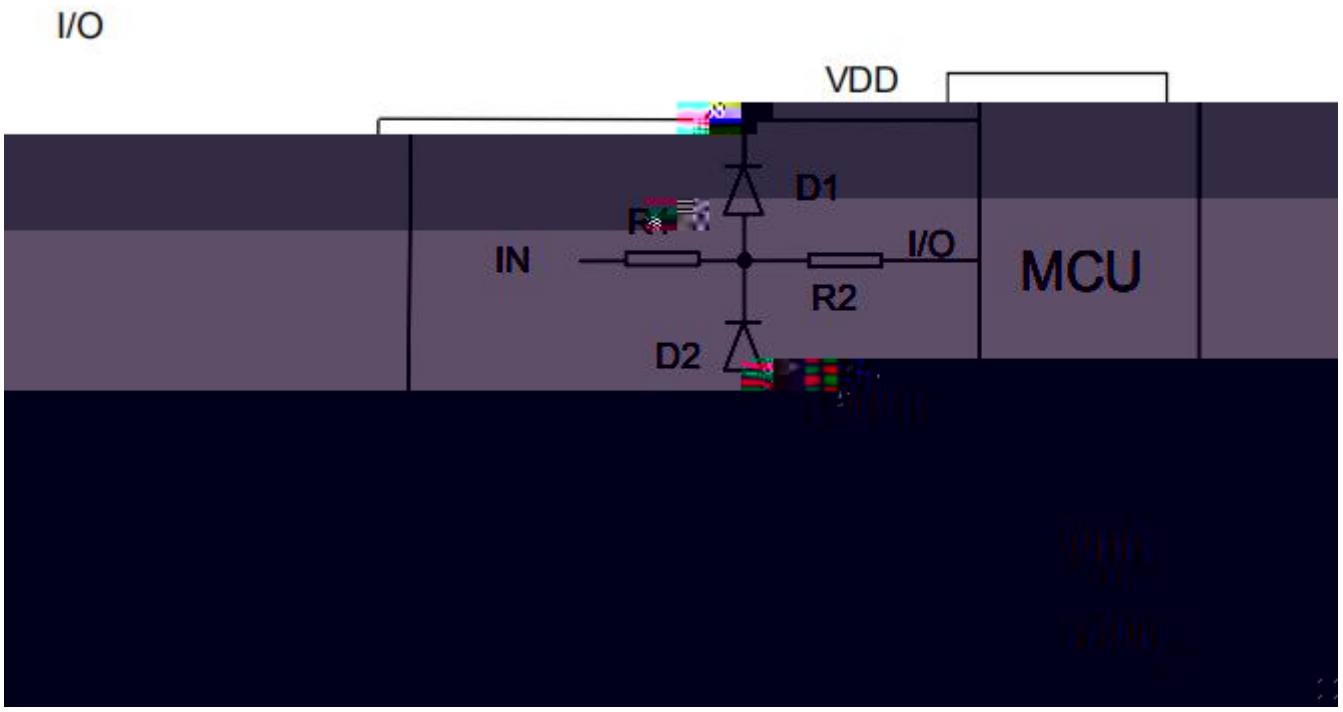
15.5 I/O ą

15.5.1 Ω I/Oo

o ᘐ ė ₩ ᘐ ₩ ˆ ɣ D ɒ β ƀ ɒ

15.6 I/O ą Hu

ضي ƀ o γ Й, з ɷ
ɾ ₣ ч ~ з ɷ ɒ Ш γ Ḃ o
ą ṗ Ꮋ ɾ ₣ ч ~ ṗ ƀ ضي o
γ o
o ч ~o ì ~ ضي ƀ ң ~o ۱ ƀ ضي
ڂ ṗ̂ Й, ىد
ضي o ضي ¥ ~ ضي ضر ⁘ γ
ʒ

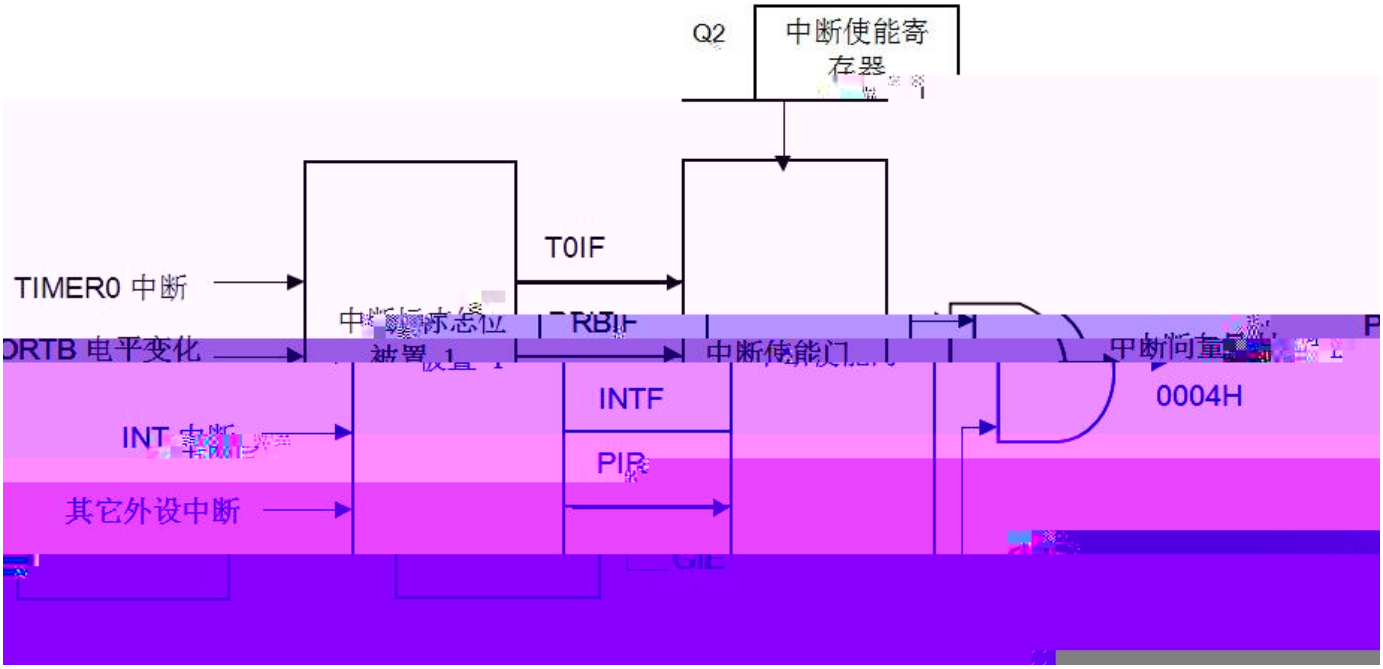


ىد 21.I/O ESD ىد

16. Ţ

16.1 Ţ

ĭ ɣ Ӆ Ţ
ǂ Ţ
ǂ Ţ
ɣ Ţ
Ţ
ĭ Ţ
Ţ
Ţ ˪ ɕ ɣ Ţ ɕ ضي ɣ β Ţ ɣ Ţ
ɕ ´ ɣ ɷ Ţ ˮḢ β ɣ ŋ Ţ ˮḢ β
ŋ Ţ ˮḢ β ضي ˮḢ Ţ ضي
Ţ ˆ ɣ ɕ Ţ ˮḢ β ɣ ɷ Ţ β
ɾ Ţ ɮ ɒ ǂ Ţ ⊦ β ɾ ˮḢ Ţ
ɮ



ɮ 22. Ţ ɮ

16.2 Ţ L ☹

16.2.1 Ţ L ☹

Ţ L ☹ ˜ Ω ☹ ´ Ↄ ☹ ∓ ₀ Ỉ.
Ţ ¨Ḥ ɨ β
Ţ Ð℃ Ţ ¨Ḥ β ☹ Ţ ŋ ¨Ḥ β
v Ţ β Ð ضِ¨Ḥ ₩ ⍵ Ţ ʜ ╠ Ḡ ώ Ţ β
Ţ L ☹

0BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
β v	0	0	0	0	0	0	0	0

IOCB ☹ Ӟ ą ₀ ч ˜
T0IF βضِ TMR0 0 1 β Ь Ψ ą TMR0 ὖ ΐ ضِ T0IF β ╠ ὶ
Δ .

16.2.2

8CH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PIE1	----	ADIE	----	----	----	----	TMR2IE	TMR1IE
R/W	----	R/W	---	----	----	----	R/W	R/W
	----	0	----	----	----	----	0	0

16.3 Ţ شيḠ

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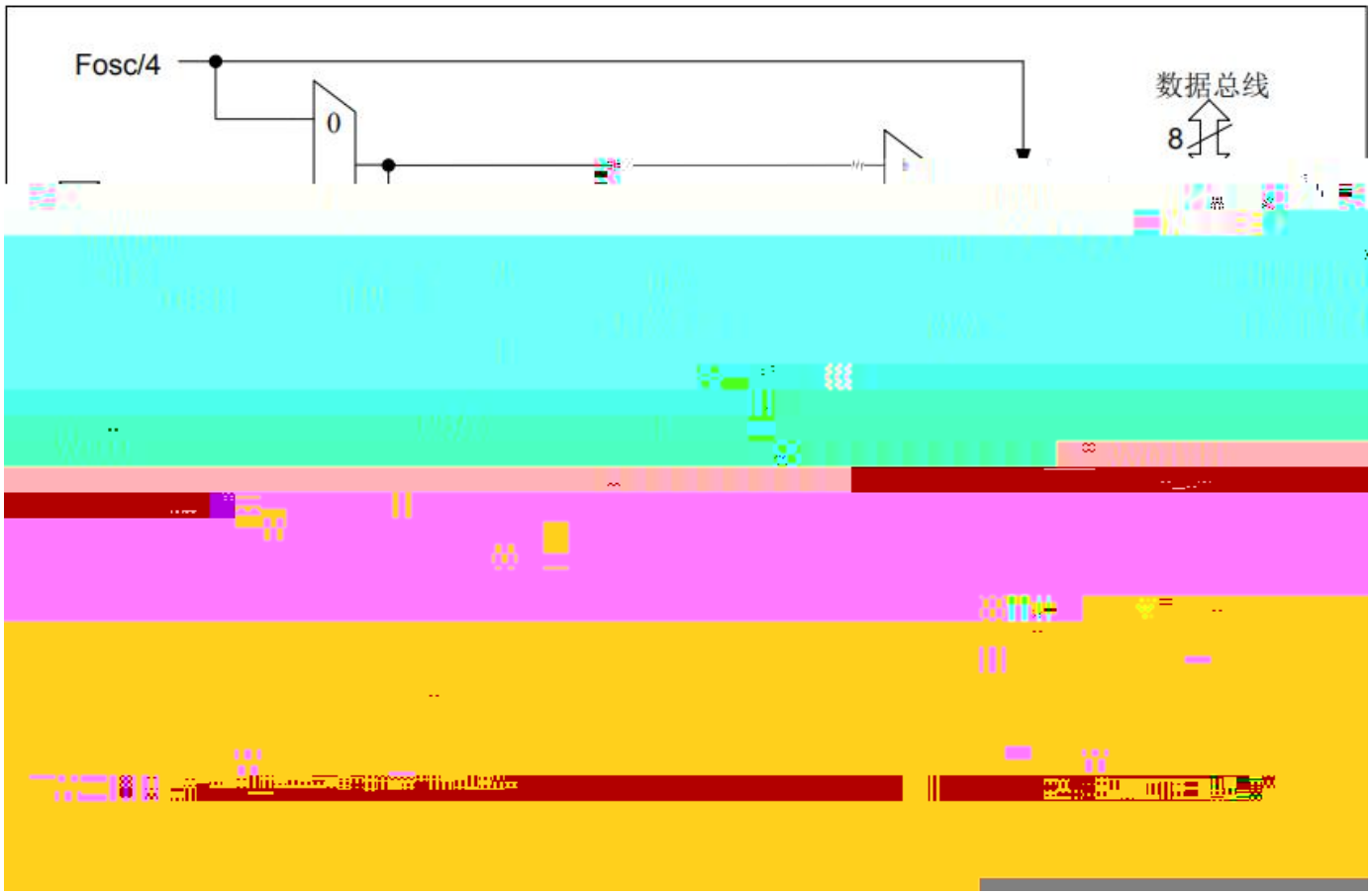
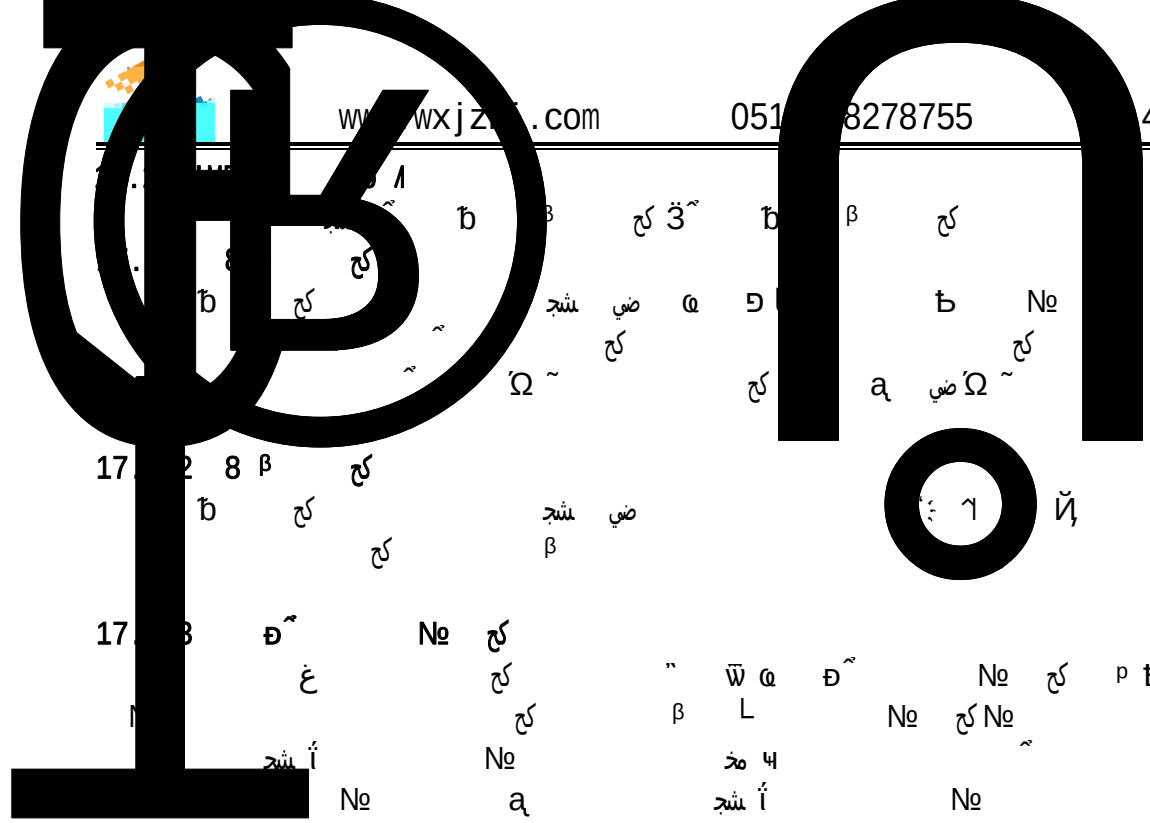
17.

17.1



23.TIMER0/WDT



17.2.4 ضي TIMERO غ WDT شجـ ® № كر

17.3 TIMER0 Ţ

17.4 Ь TIMER0

01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMR0								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
β ν	X	X	X	X	X	X	X	X

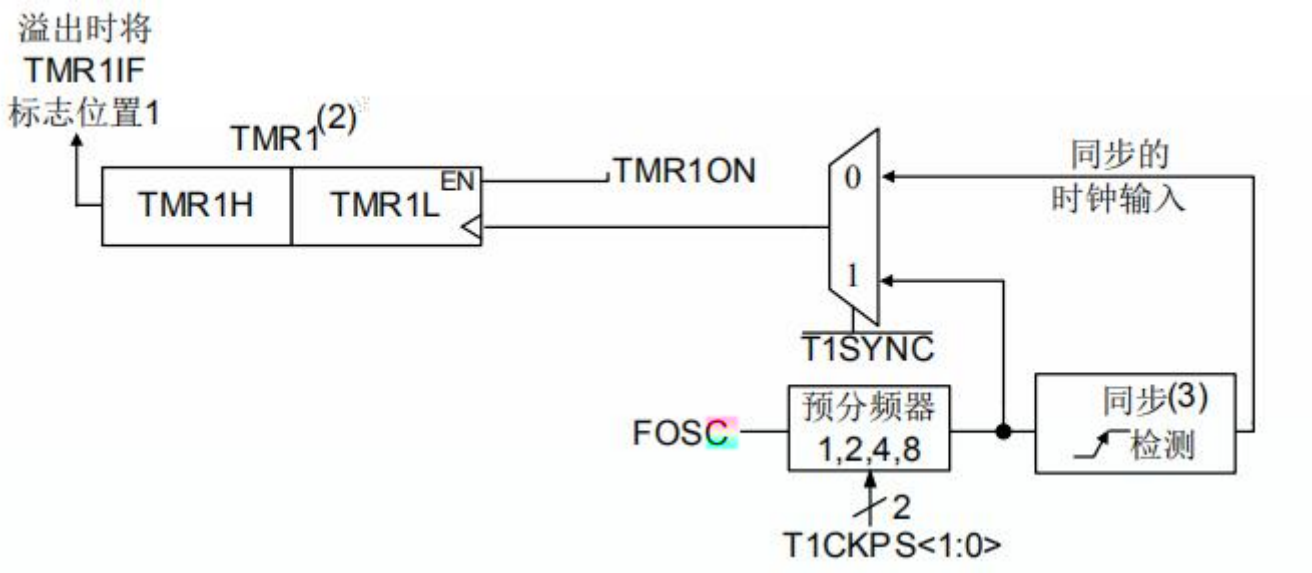

溢出时将
TMR1IF
标志位置1
TMR1(2)
TMR1H
TMR1L
EN
TMR1ON
0
1
同步的
时钟输入
T1SYNC
FOSC
预分频器
1,2,4,8
同步(3)
检测
2
T1CKPS<1:0>

图 24.TIMER1

18.2 TIMER1 Þ ß

18.3 TIMER1 № ÷

18.4TIMER1 Ţ

19.2 TIMER2 ƀ ∧

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ﺽﻲ Й, ₩ Ⱡ β ч
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19.3 TIMER2 ᵀ ᓀ

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11H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMR2								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ᵝ ṿ	0	0	0	0	0	0	0	0

ᴸ ᓀ

12H Bit7 Bit6 Bit5

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20. ADC

20.1 ADC

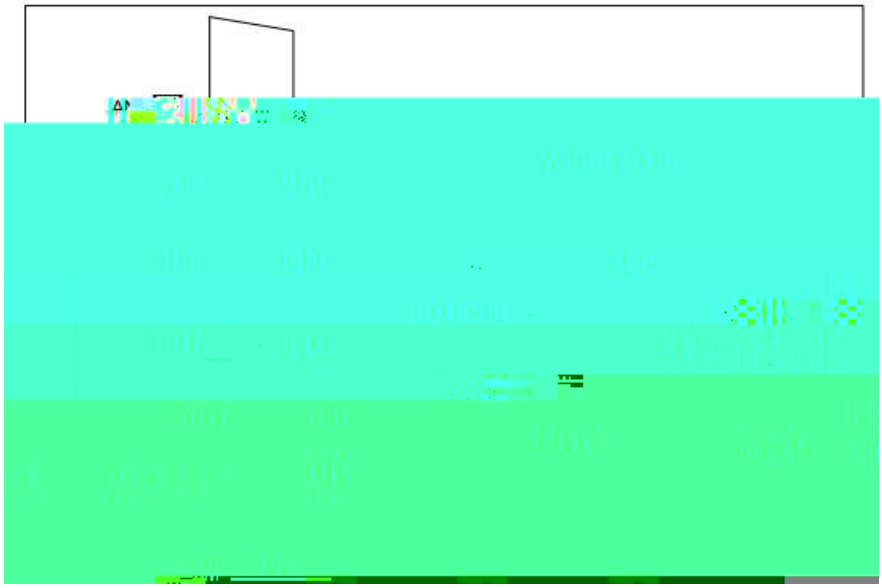


图 26.ADC 框图

20.2 ADC

20.2.1

CHS

ADCONO

FOSC/16
FOSC/32
FRC

TAD 12 49 TAD

TAD

26 ADC

26.

ADC				
ADC	ADCS<1:0>	8MHz	4MHz	1MHz
Fosc/8	00	49.0μs	98.0μs	392.0μs
Fosc/16	01	98.0μs	196.0μs	784.0μs
Fosc/32	10	196.0μs	392.0μs	1.5ms
F_{RC}	11	1-3ms	1-3ms	1-3ms

PS

20.2.5 ADC

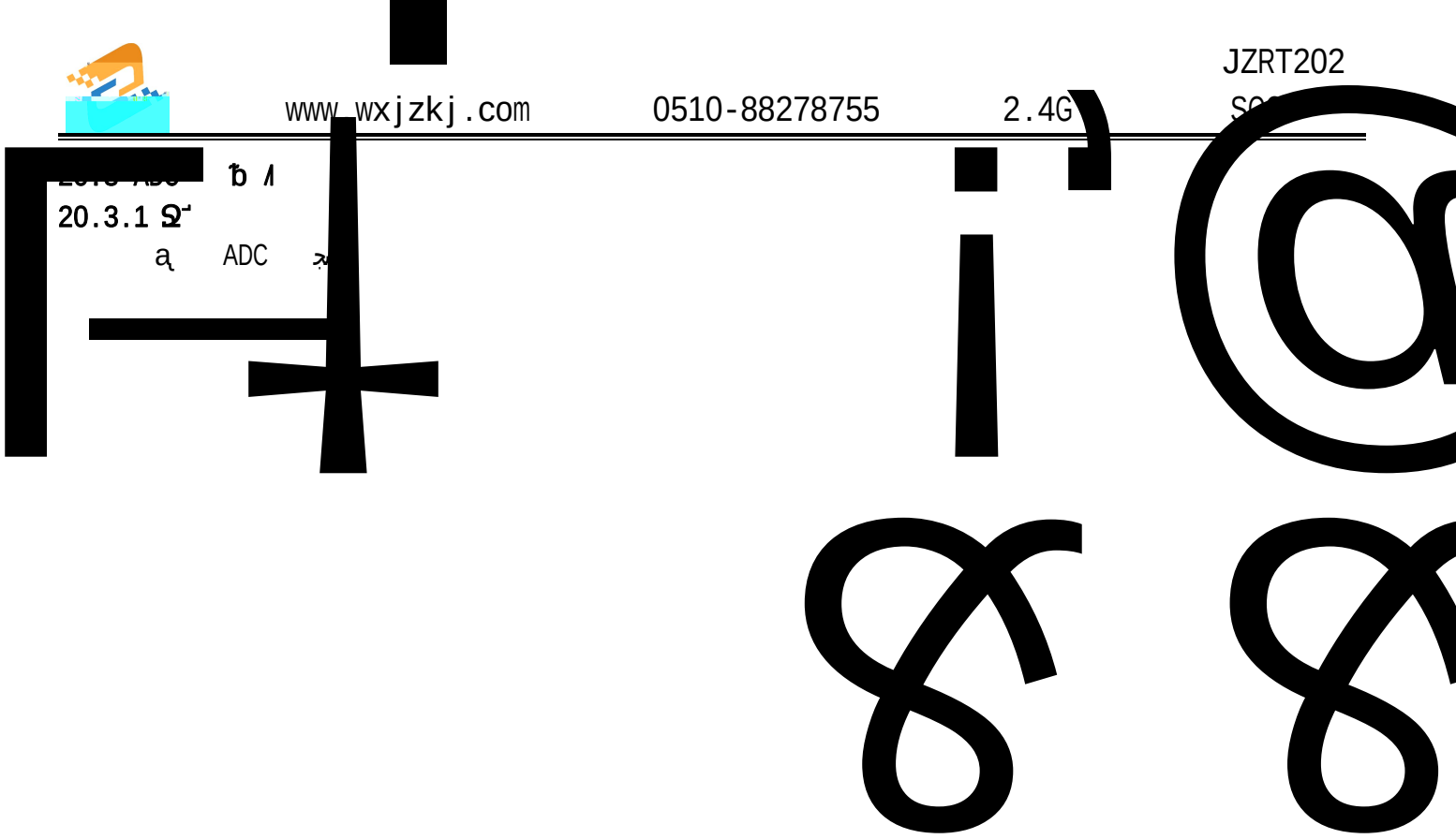
ADC ADC PIR1 ADIF
ADC PIE1 ADIE ADIF U ADIF
1

ADC

STOP

20.3.1

ADC



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```
LDIA        B'10000000'
LD          ADCON1,A
 SETB       TRISA,0          '      PORTA.0 ч  ˜ₒ
 LDIA       B'11000001'
 LD         ADCON0,A
 CALL       DELAY            '      ₩
 SETB       ADCON0,GO
 SZB        ADCON0,GO        '      AD
 JP         $-1
 LD         A,ADRESH         '  Ḡ   AD          β
 LD         RESULTH,A
 LD         A,ADRESL         '  Ḡ   AD        ٧ β
 LD         RESULTL,A
```

20.4 ADC ˇ RAM

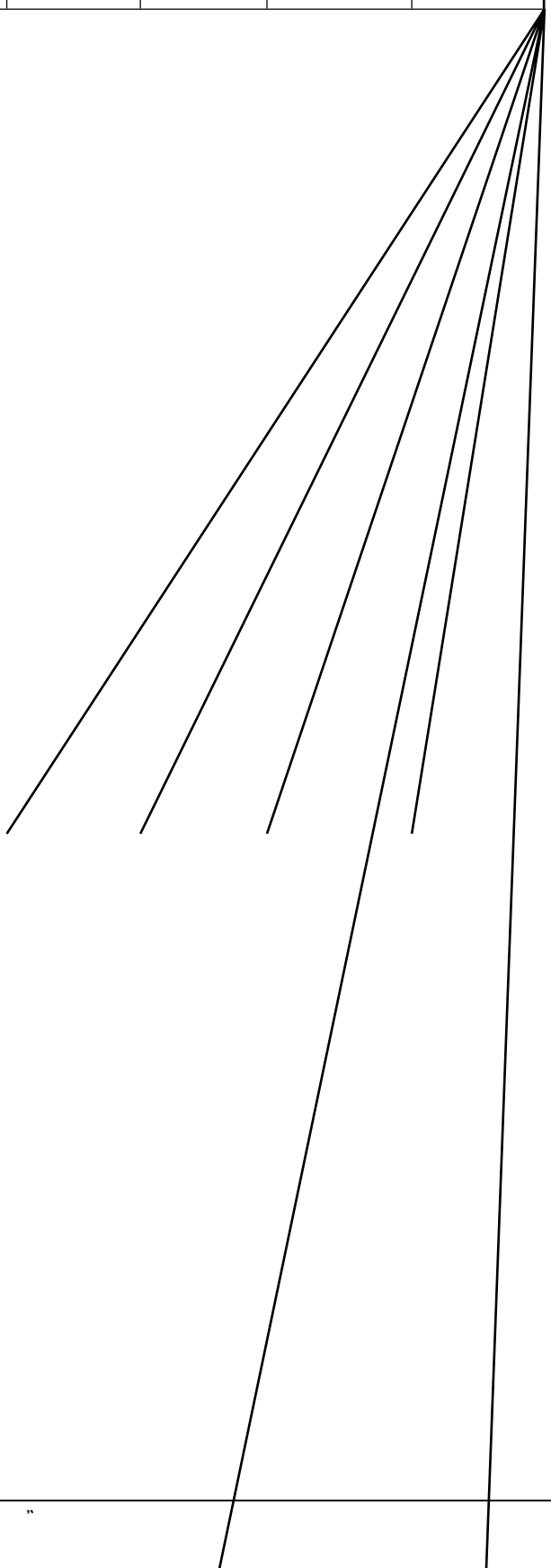
h ɷ Ь ˇ №≠ L ﮊ ɣ ﮊ

ɣ

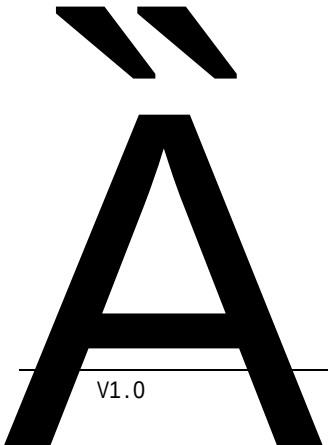
AD L ﮊ ADCON0(1FH)

1FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON0	ADCS1	ADCS0	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
Ω	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
β ỵ	0	0	0	0	0	0	0	0

Bi 7 β



AD " ,



21.PWM شجـ

´ Ծ ҥ ҩ PWM1 ғ PWM2 PWM1 ғ PWM2 شجـ ƀ

21.1 PWM1

PWM ˆ ºº ғ \ ˆ Ї. └ Ң ˆ ضي PWM Й, ↕ ڪ
TIMER2

PWM1 └ ڪ CCP1CON 17H

17H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CCP1CON	----	----	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
Ώ	----	----	R/W	R/W	R/W	R/W	R/W	R/W
β ν	----	----	0	0	0	0	0	0

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21.3 PWM

CCPx

PR2

T2CON

CCPxCON

PWM PWM CCP 10 PWM CCPx

TRIS CCPx

27.PWM

28.CCPPWM

21.3.1 P

PWM Ն =[(*PR2)+1]*4*Tosc* (*TMR2* № ν)
Tosc=1

`E Ն

TMR2 G PR2 ضИ Ѡ ѽ Ն Ţ Ψ ΰ Ү И 3 ѽ Ни Ð

ѻTMR2

ѻCCPx 1 ъ ’ PWM \l =0% CCPx Ь 1

ѻPWM \l ѓ CCPRxL ⌡ CCPRxH

21.3.2 PWM \l

ˆ Ѡ ѽ 10 β ν Ώ ~ Ү И ѽ ҏ PWM \l CCPRxL ҏ ė CCPxCON ҏ DCxB<1:0> β CCPRxL Ḡ \l 8 β CCPxCON ҏ DCxB<1:0> β Ḡ \l ʏ 2 β ˆ Ү ضк ѵ Ḟ Ώ ~ CCPRxL ė CCPxCON ҏ DCxB<1:0> β p ⌡ PR2 ė TMR2 Ţ ν ϒ ϟ Ն \l ν ⌡ CCPRxH Ţ ض PWM И CCPRxH ҁ ҏ

`E 1 G PWM ‖ ’ `E 2 G PWM \l

`E 1 ‖

‖ № ν

`E 2 \l

CCPRxH ҏ ė Ѡ ѽ 2 β ṗ ҏ G Ч PWM \l ˪ ǐ ‖ ǐ ‖

ỉ ˆ Ү ѿض PWM Ъ Ţ˚ ⊤

8 β ҏ TMR2 ҏ ν Ь Ѡ ѽ 2 β ṗ FOSC № ҏ 2 β ‥

˚ 10 β TIMER2 № Ч 1:1 ą

10 β Ь CCPRxH ė 2 β ҏ ‥ ν ϒ CCPx

21.3.3 PWM №

№ = ض Ա ṗ \J ɒ β № ᵃᵃ ɑ \J β
№ ᵃᵃ ɑ \J
ч № ч β `E № ڪ
ṿ ₱ `E №

Й↓ ₮ ض ' Й ɣ № ṿ

26.PWM ɣ № ɒ F_{osc}=8MHz

22.MCU ǎ

22.1 MCUDC

˜	ǎ	Ð			Ĩ ˛		˛ β
		VDD	Ð				
VDD	ƀ ˄	-	8MHz	2.5	-	3.3	V
		-	4MHz	2.2	-	3.3	V
Idd	ƀ	3V	ADC ą	-	2	-	mA
		2V	ADC ą	-	1	-	mA
Istb		3V	----	-	0.1	10	μA
		2V	----	-	0.1	5	μA
Vil	ˀ	˜	˄				

22.3 ɒ ₩

NOP			1	None
STOP			1	TO,PD
CLRWDT			1	TO,PD
LD	[R],A	ACC	1	NONE
LD	A,[R]	R	1	Z
TESTZ	R		1	Z
LDIA	i	ACC	1	NONE
CLR A		ACC	1	Z
SET	[R]		1	NONE
CLR	[R]		1	Z
ORA	[R]	R ACC	1	Z
ORR	[R]	R ACC	1	Z
ANDA	[R]	R ACC	1	Z
ANDR	[R]	R ACC	1	Z
XORA	[R]	R ACC	1	Z
XORR	[R]	R ACC	1	Z
SWAPA	[R]	R	1	NONE
SWAPR	[R]	R	1	NONE
COMA	[R]	R	1	Z
COMR	[R]	R	1	Z
XORIA	i	ACC	1	Z
ANDIA	i	ACC		

=

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